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Development of a Lower Power 5.12 Gbps Data Serializer and Wireline Transmitter Circuit for VeloPix Chip

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We report on a prototype of a 5.12 Gbps Data Serializer and Wireline Transmitter circuit in 130 nm CMOS technology. A shift-register-free topology has been used in the serializer block. A 16-to-1 multiplexer selects one bit of data at a time from either a posedge triggered section or a negedge triggered section of a 16-bit input register clocked at 320 MHz. The serializer consumes only 15 mW of power and the wireline transmitter with pre-emphasis consumes 45 mW. The authors will explain the circuit design aspects and present experimental results.

Summary

The LHCb collaboration has planned an upgrade of the VELO detector for the Long Shutdown 2 (LS2) period [1]. The frond-end readout electronics requires significant modification to operate at the hit rate which is a factor of 10 above that at present. A group of ASIC designers from Nikhef (Amsterdam) and CERN work on a new front-end readout chip in 130 nm CMOS technology called VeloPix [2] which is based on Timepix3 chip [3] .

In the hottest region of the detector each VeloPix chip (2cmˆ2) will deliver more than 15 Gbit of data per second. The data in the form of 128-bit frames will be routed to one of four output blocks (4 x 5.12 Gbps). A frame consists of four 30-bit data packets, 4 parity bits and a 4-bit header. The data frame will be serialized to a single-bit stream for transmission over a low-mass (lossy) copper cable. The serialization allows to minimize the number of interconnects and thereby reduces the amount of material. The transmitted signals will be distorted in the lossy cable so pre-emphasis is required to improve the signal quality at the receiver side.

Before the serialization the data packets will be encoded (scrambled). The parity bits and the header will not be encoded to provide low-level data error detection and frame alignment. After scrambling the data will be transferred to a 2 x 8 bit double data rate (DDR) register at the input of the serializer synchronous with a 320 MHz clock.

This work reports on the design and characterization of a prototype (2mm x 1mm) of the output block manufactured in a MOSIS MPW run. We test a novel byte-interleaved topology of the serializer. A Delay-Locked-Loop (DLL) generates a 16-phase select signal (16 x 195.3 ps) from a 320 MHz clock for a 16-to-1 multiplexer serializing the data stored in the DDR input register. The DLL is designed to guarantee sufficiently low jitter and mismatch between the phases (˜ 40ps p-p) and proper timing in the dual-edge clocked system. The multiplexer uses only balanced 2-input NAND/NOR gates and has uniform input-to-output delays (mismatch ˜ 13 ps p-p) . The proposed topology excludes any energy hungry circuits like shift registers and therefore consumes only 15 mW of power. The DLL is known to be sensitive to the phase noise of the reference clock. In the prototype there will be two options to investigate this : we can either supply an external reference clock or supply the clock from an on-chip PLL circuit [3].

The wireline transmitter has a 3x current-mode logic (CML) buffer structure. The differential output impedance (2 x 50 Ohms) matches to the characteristic impedance of the cable. A pair of ac-coupled CMOS buffers provides a parallel signal path boosting the high-frequency segment in the output signal and thus implementing pre-emphasis functionality.

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