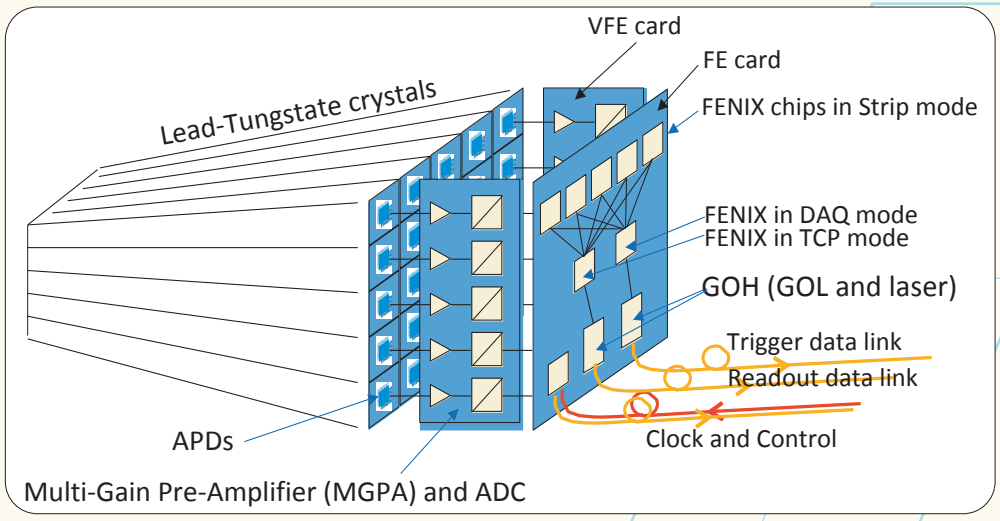
CMS ECAL Barrel electronics developments for HL-LHC

Magnus Hansen, CERN, on behalf of the CMS collaboration

The Compact Muon Solenoid (CMS) was designed to record highest quality experimental data during 10 years and 500 fb^{-1} integrated luminosity at a peak rate of $1*10^{34}$ cm^{-2}. During the High Luminosity LHC (HL-LHC) era CMS will receive an additional 2500 fb^{-1} of integrated luminosity at a levelled peak rate of $5*10^{34}$ cm^{-2} delivering significantly more data for analysis provided that:

- **1) The CMS detectors can maintain physics data quality at the higher hit density (pile-up).**
- **2) The CMS detectors can maintain physics data quality without significant degradation due to aging and radiation damage.**
- **3) The CMS trigger is capable of selecting events at maintained efficiency within a limited latency, targeting 12.5 microseconds (legacy 3,2 us).**
- **4) The CMS data acquisition system is capable of recording events at sufficient level 1 trigger rate, targeting 750 kHz (legacy 100kHz).**

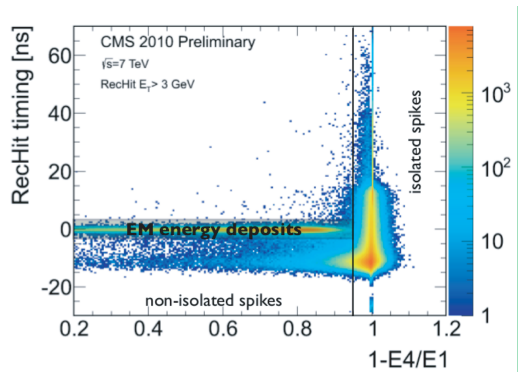
The CMS ECAL barrel electronics upgrade is planned for the LHC long shutdown 3 and is motivated to some extent by requirement 1) but essentially by 3) and 4). The 61200 Lead Tungstate ($PbWO_4$) scintillating crystals and their photodetector (Avalanche Photo-Diodes, APD) will perform until the end of the HL-LHC era.



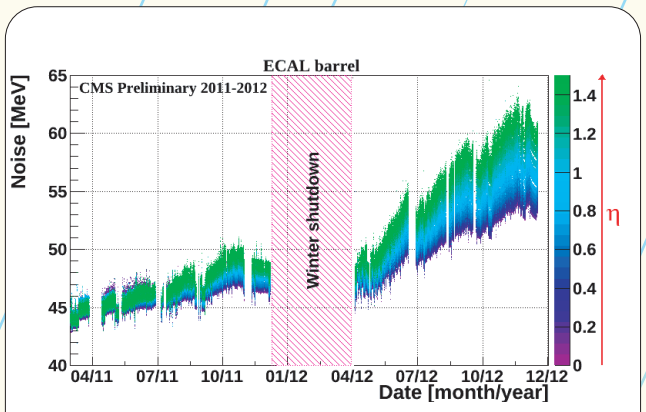
Legacy system (left): Key parameters and features

- **L1A Pipeline in Front End; max 256 LHC clocks**
- **Primary event buffer in Front End; max 25 events of 10 time samples**
- **Trigger Primitive generation in Front End; 5X5 crystal granularity**
- **On average three Data and Control fibers per 25 channels**
- **130 ASICs of 11 different designs, all 0.25um rad tol CMOS**
- **10 rad tol Linear Voltage regulators**
- **Fast and Slow control through token ring**
- **Shaping time and resolution optimized for LHC parameters**
- **Ad Hoc anomalous event filtering for the level 1 trigger**

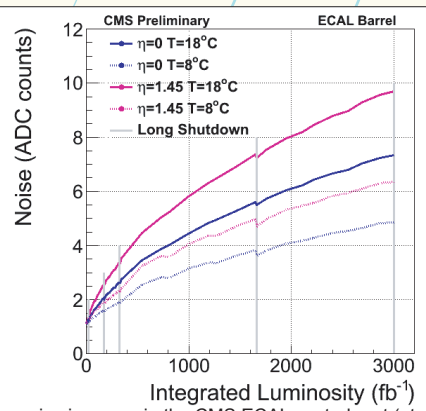
The legacy electronics system used, in addition to ASICs specifically developed for the CMS ECAL, some components developed for the CMS silicon tracker (e.g. fast and slow control, optics) and some more generic components (e.g. Gigabit Optical Link (GOL), LHC Voltage regulators)



Hit timing versus a typical shower shape variable used for spike discrimination (ratio of the energy deposit in the 4 most energetic crystals (E4) and the central one (E1))



Noise evolution for the APDs installed in the CMS ECAL during data-taking of 2011 and 2012. The noise increase is due to the radiation-induced increase in APD dark current.



Prediction of the noise increase in the CMS ECAL central part (eta=0) and lateral part (eta=1.45) if operated at room temperature (T=18 degrees C) or at lower temperature (T=8 degrees C).

Additional Issues to be addressed by the Electronics upgrade

i) Filtering of Anomalous events for the CMS trigger

Anomalous events (spikes) are energy deposits directly into the bulk of the APD and thus:

- **a) are deposited in a single APD as opposed to an EM shower that spreads laterally over several crystals (<95% in the centre crystal)**
- **b) arrive somewhat earlier than an EM shower that need to scintillate and propagate through the crystal**
- **c) are somewhat shorter than an EM shower pulse**

The plot above left suggest that a very large fraction of anomalous events are detectable in real time using dedicated hardware in the very front end and in the back end system.

ii) Compensate for increased APD noise due to radiation damage leading to increased dark current (plot above middle)

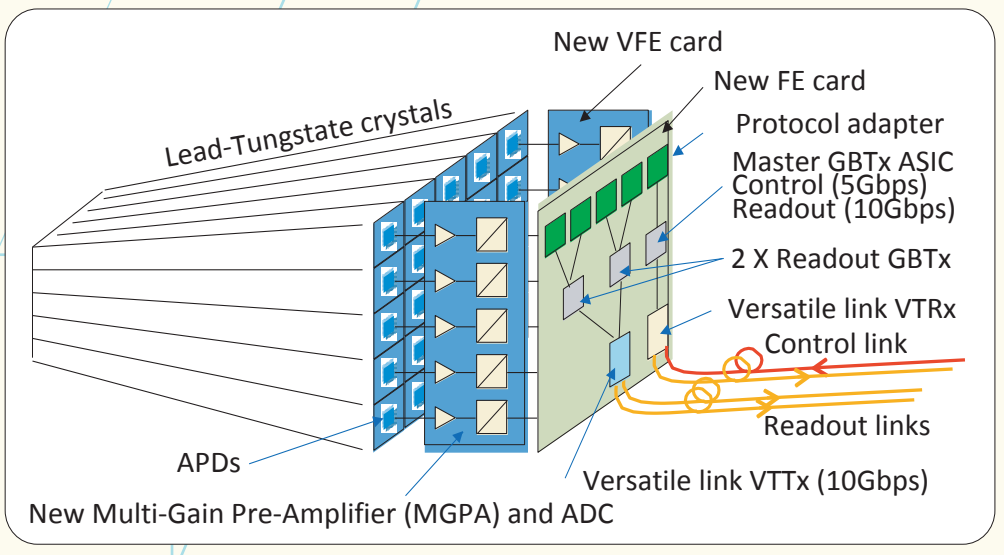
- **a) re-optimize the parameters for the pre-amplifier**
- **b) study the feasibility to operate the ECAL barrel at lower temperature**

Studies (plot above right) and extrapolation show that the APD noise can be decreased by almost a factor of two if the ECAL barrel can be operated colder than ambient temperature (8 degrees C under study). The possible gain from re-optimization of the shaping time is also under study and results are promising. Shortening the shaping time of the pre-amplifyer would also help mitigation of the out of time pile-up.

Upgraded system (right): Key parameters and features

- **L1A Pipeline in Back End; arbitrary trigger latency**
- **Primary event buffer in Back End; arbitrary buffer size**
- **Trigger Primitive generation in Back End; 1X1 crystal granularity**
- **On average four Data and Control fibers per 25 channels**
- **Fewer ASIC designs, targeting 130nm and 65nm rad tol CMOS**
- **Few rad tol switching regulators, lower power consumption**
- **Fast and Slow control link per 25 channels**
- **Shaping time and resolution optimized for HL-LHC parameters**

The upgraded electronics system will, in addition to CMS ECAL-specific ASICs, use a significant fraction of generic components (e.g. 10Gbps GigaBit Tranceiver (GBTx) and Versatile link, rad hard switching regulators) issued from current and future common projects. In addition, collaboration will be sought in order to develop and use a common hardware platform for the back end system, the ultimate goal being to limit the number of hardware designs in CMS.



Conclusion

The CMS ECAL electronics system is performing to specification but as the HL-LHC is planned to deliver significantly higher instant luminosity important adaptations are required. The legacy front-end electronics does not meet expected trigger requirements in the increased pile-up environment at the HL-LHC.

The current software solution to reject anomalous signals from the APDs could be implemented in a new electronics system.

Major functions currently implemented in the front end electronics will be moved off-detector allowing to employ cost effective Commercial Off The Shelf (COTS), like FPGAs, in the back end providing important improvement in flexibility for further algorithm upgrades.

Contact: Magnus.hansen@cern.ch; CMS ECAL upgrade project: francesca.cavallari@cern.ch. colin.philip.jessop@cern.ch