The CMS Level-1 Calorimeter Trigger Electronics System for the LHC Run II

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ABSTRACT: The CMS experiment has implemented a two-level online selection system. The first level is based on coarse information coming from the calorimeters and the muon detectors while the High Level Trigger combines fine-grain information from all sub-detectors. During Run II, the goal is to maintain the current thresholds (e.g., for electrons and photons) and improve the performance for the selection of taus. The plan to upgrade the CMS trigger system is presented as well as recent hardware and firmware developments. Algorithms selecting electrons, photons, taus and jets are also presented along with the expected performance.

KEYWORDS: Compact Muon Solenoïde (CMS); CMS trigger upgrade; Level-1 calorimeter trigger.

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1. A new electronics architecture

1.1 Goals

The new specifications of the LHC for Run II are: an instantaneous luminosity of $10^{34}cm^{-2}s^{-1}$ and an average number of pile-up events of 50. Without any modifications to the L1 electronics system, which operates with a total bandwidth of 100 kHz, the physics thresholds would have to be increased causing a severe loss of efficiency. In order to maintain low thresholds, preserve the signal efficiency and reduce the trigger rate in a high luminosity environment, the rejection power of the selection algorithms must be enhanced along with the physics object identification and pile-up mitigation. These goals can be achieved by the implementation of a new electronics architecture with high bandwidth and fast computing capabilities. High data bandwidth will permit a global view of the calorimeters at a level of the trigger towers thus improving the energy and angular resolutions.

1.2 Solutions

Currently, FPGA devices have evolved to exhibit very large programmable matrix elements, large numbers of serial links with speed up to 13 Gb/s and include complex arithmetic operators. Hardware architecture with FPGA of such performance is planned to be deployed in two scheduled stages of the CMS trigger. Newly installed optical link boards (4.5 to 6.4 Gb/s), replacing the existing copper cables (1.2 Gb/s), will be used to transmit detector primitive data to the new trigger system. Its architecture is based on two layers of MicroTCA electronics cards designed by CMS collaboration members. The Stage-1 trigger, with minimum hardware modification of the existing L1 trigger system, is mainly constructed for running the first year of

LHC Run II. The Stage 2 includes a full installation of the Layer-1[3] and Layer-2 parts of the newly L1 trigger system. It is meant to run in parallel to the Stage-1 in order to commission the system before it is used as default trigger in 2016. The data collected will be used to study the performance and optimize its operations. This architecture implements the first dedicated "Time Multiplexing Trigger" (TMT), an original solution adopted by the CMS collaboration.

In the TMT architecture, the Layer-1 cards (CTP7) are used for data formatting and pre-processing covering regions of the calorimeters. A total of 36 CTP7 are employed and each of them sends their data to each card installed at Layer-2. The Layer-2 cards (MP7) have access to the full calorimeter at trigger tower level on a single FPGA based computing device via a large number of optical serial links (72 inputs and 72 outputs). A MP7 board receives data of one bunch crossing (BX) and performs the reconstruction and identification of physics objects. Another MP7 receives data of the next BX and so on. After ten BX, the first card MP7card is again ready to receive new data. The processing time of 10 BX (25 ns) is available by the use of a pipeline. Output trigger data are then sent to the Global Trigger (GT), which also receives data from another subdetector (muon system, future track trigger) and takes the final decision. Given the required performance of the trigger, a set of 10 MP7 is enough to implement the TMT protocol.

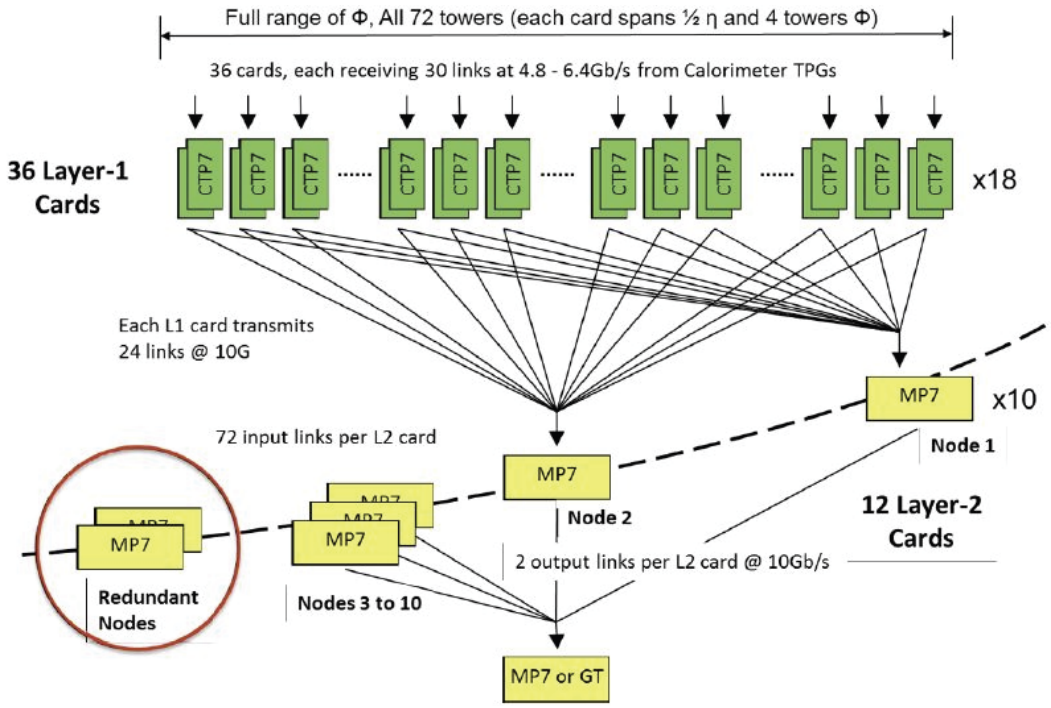

Figure 1: TMT architecture for Trigger upgrade. Two output links from each CPT7 are connected to each MP7 (24 output of CPT7 to cover 12 MP7). On the MP7 side 72, serial links are used to connect to 36 CPT7 boards from Layer-1.

1.2.1 Data format and data flow

A single CTP7 sends its data to one MP7 by means of two links running at 10 Gbps. Up to 4.3 BX are necessary to receive all data from both ECAL and HCAL calorimeters. Therefore, a pipeline within the FPGA is necessary to process the data at the incoming line speed. The data processing can begin on reception of the first data word. However, the data input format must

also be compliant with those specifications to give better flexibility to perform the algorithm computing steps. If 36 CPT7 are connected to each MP7 by two serial links, 72 serial links inputs are needed in total. Moreover, the ECAL and HCAL calorimeters have a granularity of 72 trigger towers (TT) in the phi direction and 28 TT in eta direction and this for each of the two halves, E+ and E-. Each link receives 32 bits of data after protocol decoding that requires then 16 bits to transport the data of one TT coming from ECAL and HCAL. A dedicated format has been adopted that mainly includes the sum of Ecal + Hcal energy values and extra words to locally compute the E and H values separately in series. It was also adopted that the E+ and E- parts are being read at the same time by slices of 72 entries in the phi direction, starting at the centre of the barrel (eta 0). By this mean, it is possible to compute the deposited energy inside a cluster in phi but also a cluster of two elements in eta within E+ and E- just after reception of first data slice. For the 32 bits received on each link, the internal computing frequency achieved is 240 MHz.

1.2.2 Data processing

Upon reception, each of the E+ and E- data slices is directed to duplicated computing elements inside the FPGA. Each TT is treated as a potential seed value of a cluster. Consequently, each basic algorithm function must be applied on each TT composing a slice in phi (72 TT). This imposes a duplication of the logic for each potential seed. This is an efficient way to achieve fast computing of the clusters but requires special attention when it comes to resource usage. This implies also the capability to write, as a concatenated view, the algorithm firmware code applied on one TT but in fact on all of them. The depth of the pipeline, which stores the adjacent slices, must be also managed in source code to access the neighbor TT and perform operations with it. Thus we can produce a very compact source code, which is however more difficult to understand.

For each algorithm, the clusters are computed by taking into account the information set by the associated algorithm. Only twelve of these clusters must be kept. Consequently, a sort process is employed. For each cluster and of course each algorithm, this process will first test a set of dedicated flags, previously stored by the algorithms and named "quality bits". If their values are as expected, the sort can be performed on the cluster energy values with all other selected clusters. The quality bits, the energy and localization information are compacted inside a word of 32 bits. These 12 selected words are merged with other words provided by the others algorithms. All of them can then be forwarded to two separate serial links, one link for the E+ and other one for the E- part of detector. These data are finally sent at 10 Gb/s to the Global Trigger system.

2. Trigger algorithm improvement

2.1 Algorithm precision

Given the capabilities of the trigger system described above, sophisticated algorithms have been developed and their performance studied on real data using a set of physics events from LHC Run 1. Electron Gamma (EG), Tau, Jets, ET and MET algorithms will be deployed at Layer 2 within the MP7. For example, several improvements in EG reconstruction are achieved by the use of a dynamic clustering of trigger towers **Figure 2**. The position of the candidates can be obtained with a precision better than the tower granularity. An additional discriminator of electrons / photons and jet signals is based on the shape of the reconstructed clusters. A more

precise isolation criterion without boundaries and independent from the level of pile-up, can be applied.

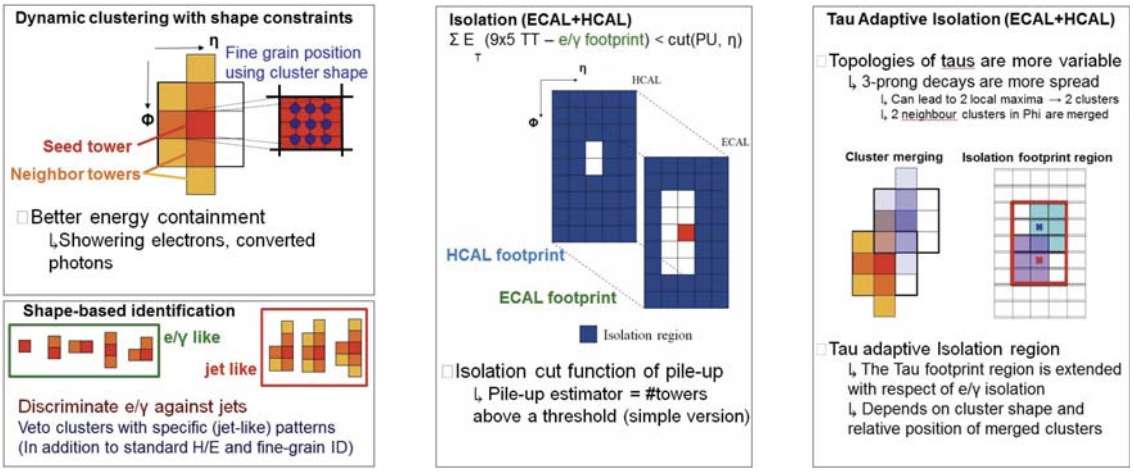

Figure 2 : EG dynamic clustering and isolation, Tau adaptative isolation

An “EG-like” cluster can be used as starting point for the Tau algorithm. After building proto clusters, secondary clusters are reconstructed in a “secondary seed searching area”. The most energetic cluster is merged with a secondary cluster to form the Tau candidate. The footprint of the merged cluster can thus be changed, which requires the use of adaptive isolation. Moreover the central position of the master cluster depends of the relative position between the main and the merged clusters. Finally a dedicated calibration scheme more complex than the EG part is applied to the Tau candidate.

2.2 Expected performances

These upgrades algorithms are tested during their development against the current ones. For the E/G algorithm, a substantial improvement by a factor 4 has been observed in position resolution, and the energy resolution is improved by about 30%. A reduction of trigger rate by a factor two is also obtained for a similar signal efficiency.

During Run1, the Tau trigger was not used as the jet trigger was used instead. An efficient identification of Tau is mandatory for the physics programme planned in Run2. If the resolution in energy is about the same in the two cases, we observe an efficiency rising to 60% of gain in the “End Cap” part of the detector and 30% in the Barrel part. An improvement of 4 is also observed in position resolution and the expected rate reduction is about 30%.

3. Firmware development at Layer-2

To implement the algorithms in firmware, the VHDL language is used. It is sufficiently sophisticated to easily support the complexity of the objects and data flow presented above and directly in line with the TMT architecture. Firmware can be classified in two main parts, the core and the algorithms. The core comprises all necessary logics that must be addressed as internals resources and accessible by software such as input pattern buffers, output spy buffers or configuration registers. The core includes also the 72 input/output optical serial links and their dedicated logic to align their data streams. The software interface is based on IPBUS standard use via firmware IP and the development software library µHAL developed at CERN.

A very efficient throughput has been measured with this protocol. This one it uses the internet media as data traffic support. The algorithm parts have been subdivided as well: Electron/Gamma, Tau, Jets, MET, ET. The UK groups have the responsibility of the Core, Jets, ET and MET algorithm sub parts, and LLR covers the EG and Tau parts. Imperial College ensures the integration of all parts to produce the downloading image of the global firmware into a XC7V690T FPGA Xilinx device. A precise floor planning scheme has been developed to efficiently perform a place and route process and to guaranty that timing constraints will be satisfied after modification of VHDL sources during the development process.

A WEB site called CACTUS has been installed as central repository structure and located at CERN. This assists the developments of the software, the firmware and keeps track of versioning via SVN . Sharing resources as well as libraries of code or documentations is also supported. This working organisation is adapted to multiple contributions from various design engineers.

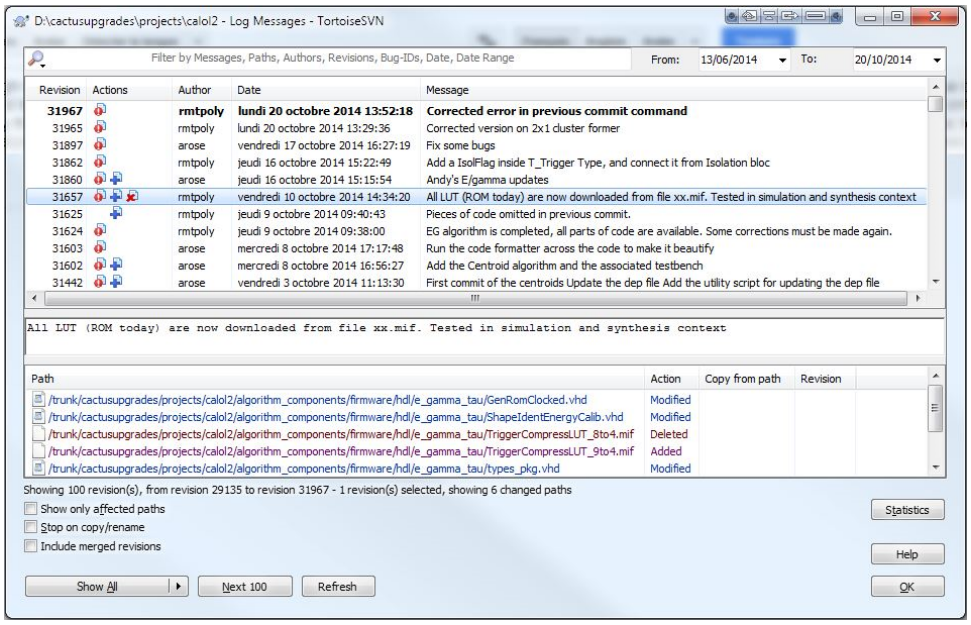

Figure 3: Electron Gamma code maintenance based on use of remote SVN at CERN

As many adders are used in the clustering part, special attention was taken to reuse these components, sharing objects or results between different sub blocks. Dedicated writing style of code can save resources or pipeline levels. The implementation of generic components is useful in such a large design relying on multi-instance and multi size concepts. Injecting specific simulated data using a test bench is a first test that is necessary to verify the functionalities of the algorithms in particular cases. But a thorough test needs to cover more cases for a correct simulation check. An automated test pattern generation and associated checks have been developed by the UK groups and shared with all designers to simulate different parts of the algorithms.

4. Physical test bench and software tools

Based on the use of the processor cards inserted in the same MicroTCA crate Figure , different parts of the firmware can be grouped or individually loaded onto a card. Pattern injection from

Layer-1 to Layer-2 and then through the Demux in order to reach the Global Trigger level can be tested at the nominal speed. Patterns can be created from a physics data set from Run I. Thus, a comparison can be done to analyse the performance enhancement of the new trigger architecture. The Trigger Timing and Control (TTC) system is used to test the synchronization mechanisms in the hardware and in the firmware. Optical harness with optical patch panel cabling, is set up as in the final installation. The real data delays between processor cards are taken into account and allow flexibility of the interconnect card or for testing several functionalities.

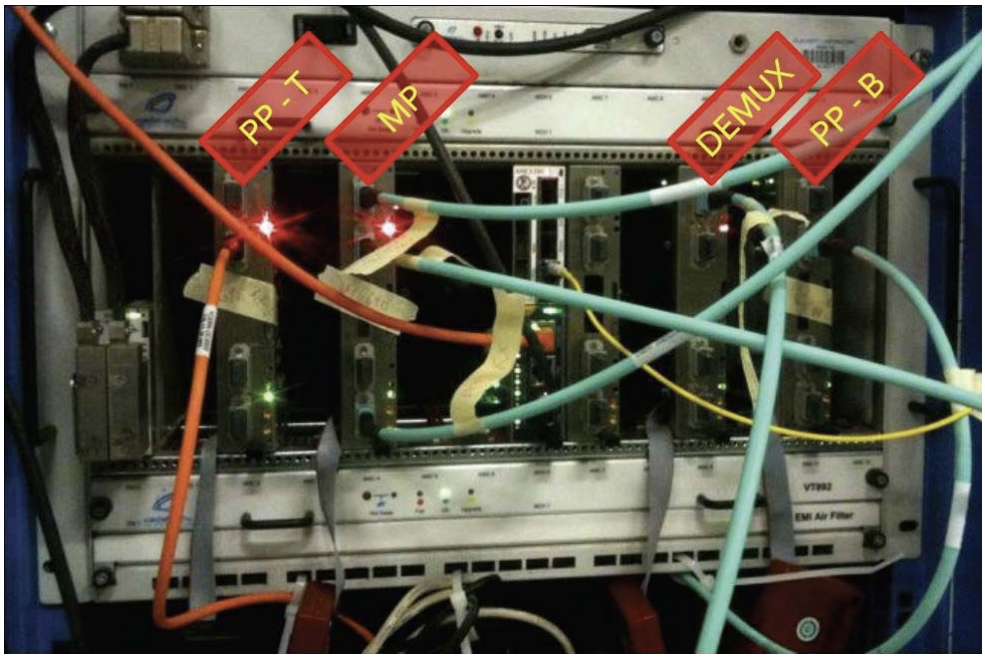

Figure 4: Layer1 and Layer2 emulator inside a same MicroTCA crate with several MP7 cards

Software tools have been developed for testing purposes. Thus the incoming or outgoing data flow can be dumped, transfers or computing control can be launched, bandwidth data flow can be measured, etc.

A software emulator for each part of an algorithm has been developed. The goal of such a tool is to compare the data delivered by the test bench to those provided by the emulator. The same set of data input is applied to the emulator and to the test bench. A software tool is also used to generate the same set of data used by the firmware engineer inside the VHDL simulator for debugging purposes. Moreover, these emulators will be inserted in the main software of the experiment. It will be useful to compare the emulated answer of the trigger system to the real data set.

5. Conclusion

An upgrade to the trigger system is requested to meet the CMS physics program. By using modern electronics technologies we have the capacity to integrate complex algorithms inside a single electronic computing device. Thereby an unprecedented level of performance can be

achieved for the trigger system, which has access to the calorimeters entirety. In parallel with the existing trigger system, this new system will be rapidly deployed with minimum risk.

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