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6 bit, Low Power SAR ADC for CBM-MUCH with Maximum Sampling Rate 50 MS/s

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The design considerations on ADCs as a building block for mixed-signal read-out ASICs in high energy physics are presented. The choice of successive approximation architecture is justified as optimal in terms of a power-speed trade-off, arising in multi-channel data acquisition systems for up-to-date physical experiments. As an example, the development of an area-efficient SAR ADC in 180nm CMOS process with variable sampling rate in the read-out ASIC for CBM-MUCH electronics is presented. The ADC power consumption, confirmed by start-to-finish design: 1.2 mW (at sampling rate 50MS/s).

Summary

The multichannel read-out electronics of up-to-date physical experiments imposes very strict power & area requirements on the application specific integrated circuits (ASICs). The main trend of new front-end chips for high-energy physics is digitalization and processing of analog signals from detectors as early as possible. So, the demand of ADC in each read-out channel arises.

To ensure the possibility of early processing in digital domain (base line correction, digital comparison, digital filtration etc.) the ADC's sampling rate has to be enough to provide 5-10 sampling points of shaper output. For example, to meet this requirement in CBM MUCH GEM chambers read-out the sampling rate over 40MS/s has to be guaranteed. The maximum available area, taking into account the size of other blocks (shapers, digital control) is $255\mu m \times 200\mu m$. The ADC power consumption is limited by few mWs.

These requirements induce the choice of successive approximation ADC architecture as optimal according to the power-speed trade-off. To meet the area constraints the split capacitor-matrix DAC can be used. Unfortunately the split of capacitor matrix with attenuation capacitor can lead to significant gain errors between sub-matrices because of the need using of capacitor not equal to unit capacitors in matrix. To eliminate these errors the increased attenuation capacitor value of two unit capacitors and error correction capacitors in LSB (least significant bit) a sub-matrix are used in proposed design. The single-ended architecture was chosen to save design area. The schematic and layout of comparator were optimized to eliminate errors arising from kick-back effect in single- ended architecture.

In the CBM-MUCH experiment it is expected that only 20% of ASIC channels will be used simultaneously, so the low power consumption in steady mode is important. To minimize static consumption the fully asynchronous architecture with an internal high speed 500 MHz clock, generated by comparator, is used. Moreover a fully dynamic comparator with near zero static power consumption is used. That makes possible to zero the ADC's consumption power in idle (no events) state. To lower the power consumption of SAR register a dynamic D flip-flop was used. That flip-flop type uses gate capacitance to store the input. Clocking at 500MHz allows to save up to 80% of power, comparing with a conventional D flip-flop, based on NAND gates.

The CBM-MUCH ASIC was fabricated in the 180 nm UMC CMOS MMRF process. ADC performance, confirmed by start-to-finish design, including post-layout simulation is as follows:
- 6 bit resolution

- Maximum sampling rate 50MS/s
- 1.2 mW power consumption at the maximum sampling rate 50 MS/s

- ADC area 255um x 100 um (0.0255 mm^2)
- maximum DNL – 0.6 LSB
- Effective number of bits at 1 MHz input – 5.4

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