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The High Throughput Readout Chain of the DSSC 1M Pixel Detector Operating in Pulsed Mode

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The readout chain of the DSSC 1Megapixel detector currently built at DESY, Hamburg for the European X-Ray Free Electron Laser XFEL.EU is described.
The system operates in a pulsed mode comparable to the new ILC. 800 images of 1Megapixels (9 bit per pixel) are produced at a rate of 10 Hz leading to a total throughput requirement of 144 GBit/s.
In order to deal with the high data rates, the latest Kintex7 FPGAs are used to implement fast DDR3-1600 image buffers and high speed Aurora- and 40 GBit/s QSFP+ links.

Summary

The DSSC camera is a 2D high-speed X-ray detector with 1M pixels built for the European X-Ray Free Electron Laser XFEL.EU at DESY in Hamburg. DSSC produces 144GBit/s of data contained in 800 images of 1Megapixels taken at a repetition rate of 10Hz.

To deal with this data rate a 2 stage data aggregation is implemented using latest technology FPGAs.
In the first stage, a space saving Spartan6 FPGA is used to bundle the data output of 16 ASICs into 3 high-speed serial Xilinx Aurora links running at 3.125GBit/s each.
These IOBoards are located close to the sensors and readout ASICs in Vacuum.
The second stage, implemented outside of the vaccum vessel, collects the data stream of 4 IOBoards. The implemented Xilinx Kintex7 FPGA contains memory controllers for large high-speed DDR3 buffers as well as one 40GBit/s QSFP+ link.
It is also the main control unit of the system.
Using a standard Ethernet link, it is possible to communicate to the Linux running on a Microblaze IP core inside the Kintex7.
4 Kintex7 boards can handle the full data rate of the 1M pixels camera.

The XFEL generates 10 bursts per second, each containing 3000 X-ray pulses spaced by 222ns, corresponding to a repetition rate of 4.5MHz.
DSSC exploits this low duty cycle by pulsing the power supplies of several electronics components.

The DSSC pixel ASICs detector can store 800 images in an internal SRAM which has to be read out within 0.1 seconds before the next burst arrives.

Each pixel value is stored as a 9bit value.
For better alignment the 9 bits are extended to 16 bits within the readout chain. This results in a data output of 144GBit/s for the whole 1M pixels detector.

The first stage collects data from the readout ASICs via one 350MHz LVDS connection per ASIC. These signals are sampled in the IOBoard-FPGA by special delay and

de-serialization logic.
After some FIFO stages the data is fed into the high speed serialisers of the aurora core.
The output rate of one Spartan6 FPGA is 7.5GBit/s. The required data rate between IO Board and PPT is 5.25GBit/s.

In the Kintex7 four data receiver modules are implemented that collect data from one IOBoard each.
Since the input data stream can not be blocked, a large DDR3-1600 buffer is used to store the data.
Its operation frequency is 800 MHz double data rate, combined with a 64bit parallel I/O data bus,
this adds up to a total data rate of the DDR3-Ram of 102GBit/s. In alternating read/write burst mode reading/writing blocks of 8KB size a throughput of 88GBit/s was achieved.
Using the DDR3 image buffer, data reordering on image level can be realized.

For transmitting the data to the external train builder module, the internal PHY of the Kintex7 is used to establish one 40GBit/s QSFP+ link.

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