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10 MGy Total Dose Evaluation of 65 nm CMOS Technology for the High Luminosity LHC Upgrades

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The radiation tolerance of the 65 nm bulk CMOS devices is investigated using 10 keV X-rays up to a Total Ionizing Dose (TID) of 10 MGy and the implications on the DC performance of n and p channels transistors are presented.

For a dose level of 10 MGy, transconductance loss is near 100% for the narrow channel pmos device making the device completely off.

Annealing at 100°C helps devices to recover driving capabilities but the threshold voltage is increased to 1 V for the narrowest pmos device reducing hence the noise margin in digital circuits.

Summary

The High Luminosity LHC is the proposed upgrade to the LHC to be made after around 2020. The upgrade aims to increase the luminosity of the machine by a factor of 10, up to $1035 \text{ cm}^{-2}\text{s}^{-1}$. The upgrade improves statistically marginal measurements and provides a better chance to see rare processes.

ATLAS and CMS experiments are planning major detector upgrades to cope with the increase in the beam luminosity. Pixel detectors are placed in the innermost part of the experiments and are therefore exposed to the highest fluences and the highest ionizing radiation. Simulations show that the new pixel detector will integrate a fluence (1 MeV neutron equivalent) of about 1016 n/cm^2 and a Total Ionizing Dose (TID) of 10 MGy.

The 65 nm CMOS process seems to be promising for the future pixel readout chips in term of high integration density but it have to be extensively tested and qualified for the irradiation.

A lot of information can be obtained by studying radiation effects on individual transistors, particularly to understand the reason of failures in digital or analog design. This is why we tested and evaluated the effect of the TID of the core transistors from 65 nm commercial bulk CMOS process. Since the dominant TID effect is the charge buildup in the STI, the parasitic transistors can be considered as the main source of degradation. This is why, devices with different sizes in plus of an enclosed geometry device layout were considered in order to study the TID effects.

First tests were done up to 2 MGy on transistors with different geometries. A 50% current driving loss was observed for the minimum size p-channel device. This tends to slow down digital circuits as observed on the ring oscillator implemented with the same process and tested up to 2 MGy.

Further testing on devices for digital design having a width varying from 120 nm to $1 \mu\text{m}$ were done up to 10 MGy and show that the leakage current degradation does not seem to be the main issue with this process. However, we observed an important performances degradation for both n and p channels devices starting from a dose level of 2 MGy and particularly for the narrow pmos devices. At a dose level of 10 MGy, the pmos transconductance loss is near 100% for narrow channel devices which makes the device completely off.

The Annealing at low and at room temperature does not really help to recover and any recovering was observed after 40 days of annealing. However, a perceptible performances recovery is allowed with annealing at 100°C for 1 week. In fact, devices recover some driving capabilities and the transconductance loss for the narrowest pmos device decreases to 40% after high temperature annealing. However, the threshold voltage is still increasing with annealing and reaches a value of 1V for the narrowest pmos device. The noise margin in

digital circuits is then significantly reduced and errors may be introduced.

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