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New Production Methods for Silicon Bare Modules for the CMS Pixel Detector, Upgrade Phase I

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This paper describes the production process and results for the fourth barrel layer for the CMS silicon pixel detector, upgrade phase I. The fourth layer will be produced in distributed detector production lab (DDTL) at KIT and DESY. Both research centers have commonly developed and investigated new production processes, including SAC solder bump jetting, gold stud bumping and precoat by powder processes (PPS) to bump the sensor tiles and prepare them for the flip-chip process. First production samples with the new digital ROCs have been produced and tested with a 90Sr source, indicating a yield of 100%.

Summary

The next CMS detector - upgrade I –is under construction. A fourth silicon detector layer will be added to the barrel. It is produced by a German collaboration between KIT and DESY. In order to accelerate the development of the bare module production processes and to reduce costs and risks a new methodical way of collaborating was chosen. Both research facilities share the production processes, hence optimizing and sharing know-how in a distributed detector package lab (DDPL). While formerly double indium bump-bonds were used, the current production processes utilize single SnPb- and SAC-solder bump flip chip technologies. This paper describes the current status of the production, testing and the production yield.

The silicon bare modules comprise of an 66 x 21.16 mm2 large silicon sensor with 16 digital readout electronic chips (ROCs) bump-bonded to the sensor. Thus a bare module has 66560 pixels and bond contacts. The solder opening on the sensor measures 30 µm, hence the requirement on the position accuracy of the flip chip process exceeds 5 µm. For the KIT production lot, the UBM and 30 µm SnPb solder balls were applied galvanically by RTI. DESY established a solder-jet process to apply SAC solder balls with a diameter of 40 µm on top of the electroless grown pad-UBM. Alternatively investigated bumping solutions include automated gold-stud bumping and precoat by powder sheet (PPS) processes. The flip-chip process is done by means of a FINEPLACER® femto with an in situ reflow chamber. The complete module is reflown under formic acid. Production tests include mechanical pull and shear tests. Additionally, the solder joints are investigated by X-ray, SEM and cross sections. In thermal tests the modules are cycled from -20 ℃ to +20 ℃.

Electrical tests include I/V and C/V sensor tests. The ROCs have been fully qualified on wafer level. Optionally, single ROCs can be tested on the FINEPLACER immediately before the bonding process. The electrical bare-module testing is done on a motorized prober station.

The production time for a complete module is about 60 minutes. Mechanical pull tests values exceed 10 kg for one ROC soldered on a single sensor, the shear values 13 cN per bump, indicating a very strong mechanically connection. X-ray inspection of the solder joints revealed highly reliable and void-free solder joints. The first production samples exhibited 100 % yield. They were tested by a 90Sr source and a X-ray tube. No bumps were missing and all pixels responded electrically as expected for both the analog and the new digital ROC. The testing time for one ROC on the module including calibration is currently about 5 minutes, but will be accelerated by new test software releases. Rework procedures foresee a single ROC to be unsoldered and replaced.

The joint efforts inside the DDPL helped both DESY and KIT to quickly install a reliable and robust production process for future pixel detector assemblies.

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