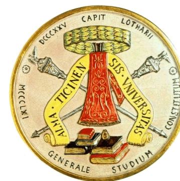
Design of bandgap reference circuits in a 65 nm CMOS technology for HL-LHC applications

Gianluca Traversi[a,c], F. De Canio[b,c], L. Gaioni[a], M. Manghisoni[a,c], L. Ratti[b,c], V. Re[a,c]



[a]Università degli Studi di Bergamo

[b]Università degli Studi di Pavia

[c]INFN

Topical Workshop on Electronics for Particle Physics (TWEPP 2014)

22 – 26 September 2014, Aix en Provence, France

Outline

- ✓ Introduction
- ✓ Bandgap reference circuit in the 65nm TSMC CMOS technology
  - ✓ Bandgap with Bipolar Transistors
  - ✓ Bandgap with diodes
  - ✓ Bandgap with MOSFETs in weak inversion region
- ✓ Bandgap components:
  - ✓ Startup circuit
  - ✓ Operational amplifier
- ✓ Simulation results
  - ✓ Monte Carlo simulation
  - ✓ Four-Corner simulation
- ✓ Prototype chip
- ✓ Conclusions and future activity

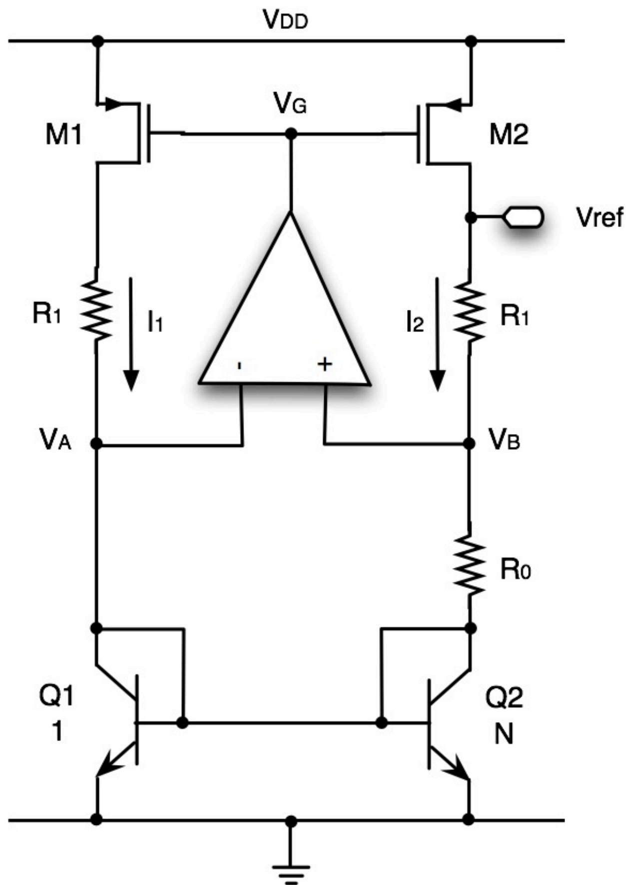
Introduction

- Voltage references are commonly used in a wide range of applications
  - Embedded in complex systems
  - As stand alone devices
- Stability against temperature, power supply and process variations
- Requirements and trade-offs
  - Output voltage precision (Trimming, Curvature compensation vs test time and complexity) -> no trimming
  - Radiation hardness -> (TID effects, displacement damage) -> problems may arise in bipolar transistors and diodes due to charge trapped in oxide above diode and to bulk damage
    - Bandgap circuits with different devices (BJTs, Diodes, MOS, MOS with EL)
  - Power consumption
  - Load current (class A or AB output stage can be included if needed)
  - Layout area

Bandgap References

- Output voltage with a low sensitivity to the temperature: combine a voltage with positive TC with a voltage with negative TC
  - Positive TC (PTAT): thermal voltage V_T=kT/q (+0.086 mV/K) at 300K
  - Negative TC (CTAT): base-emitter voltage V_{BE} (-2.2 mV/K) at 300K
- Temperature Coefficient (TC): $TC = \frac{\Delta V_{OUT}}{V_{OUT} \cdot \Delta T}$
- Reference Voltage $V_{REF} = V_{BE} + mV_T$
  - $TC \approx 0 \Rightarrow m = 25.6 \Rightarrow V_{REF} \approx 1.2$ V ($\approx V_{BG}$)
- Voltage mode bandgap circuits: $V_{REF} = V_{BE} + mV_T$;
- Current mode bandgap circuits: $V_{REF} = R\,(V_{BE}/R_0 + mV_T/R_0) = \alpha\, V_{BG}$

Voltage Mode (VM) Bandgap References



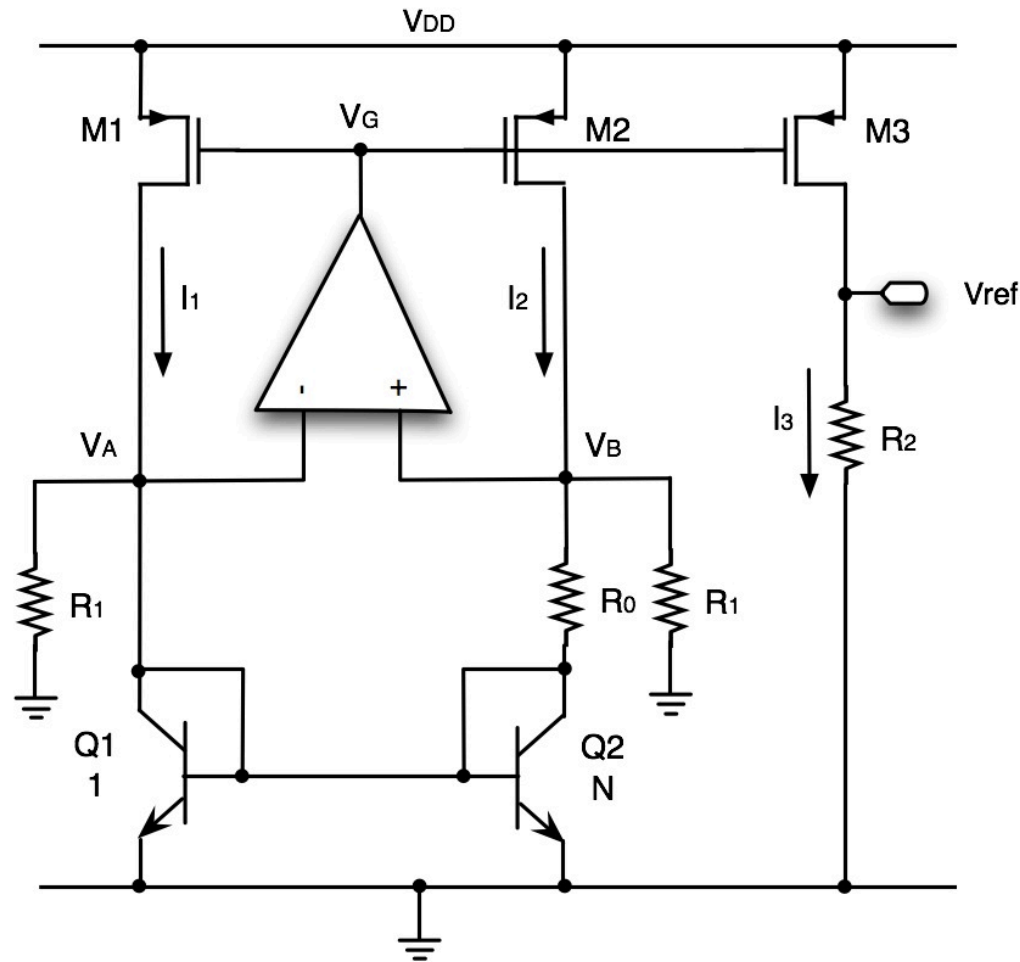
$$V_A = V_B = V_{BE_Q1}$$

$$\Delta V_{BE} = V_{BE_Q1} - V_{BE_Q2} = V_T \ln(N)$$

$$V_{REF} = V_{BE_Q1} + \frac{V_T \ln(N)}{R_0} R_1$$

$$m = \ln(N) \frac{R_1}{R_0}$$

Current Mode (CM) Bandgap References



- V_A and V_B are kept equal by the op-amp

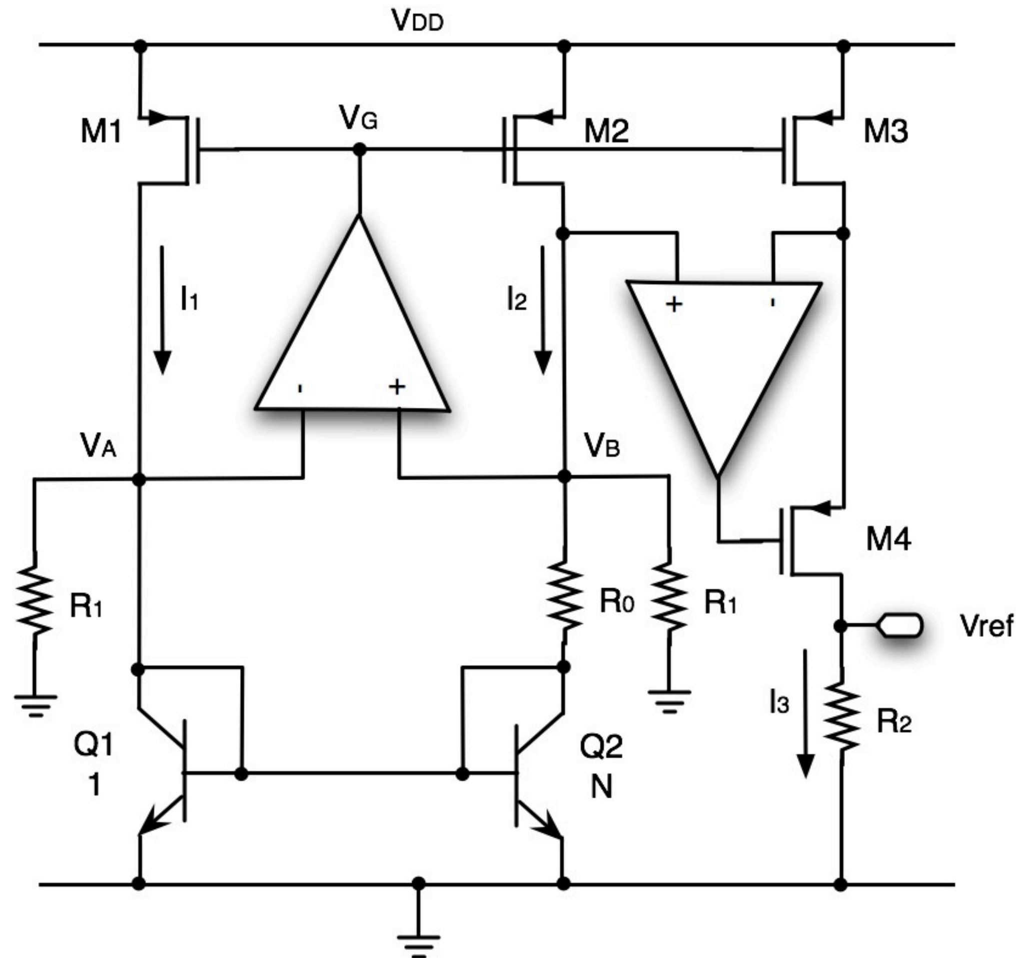
$$I_1 = I_2 = \frac{V_T \ln(n)}{R_0} + \frac{V_{BE}}{R_1} = I_3$$

$$V_{REF} = V_T \frac{R_2 \ln(n)}{R_0} + V_{BE} \frac{R_2}{R_1}$$

$$m = \frac{R_1 \ln(n)}{R_0}$$

$$\alpha = \frac{R_2}{R_1}$$

Current Mode (CM) Bandgap References



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$$I_1 = I_2 = \frac{V_T \ln(n)}{R_0} + \frac{V_{BE}}{R_1} = I_3$$

$$V_{REF} = V_T \frac{R_2 \ln(n)}{R_0} + V_{BE} \frac{R_2}{R_1}$$

$$m = \frac{R_1 \ln(n)}{R_0}$$

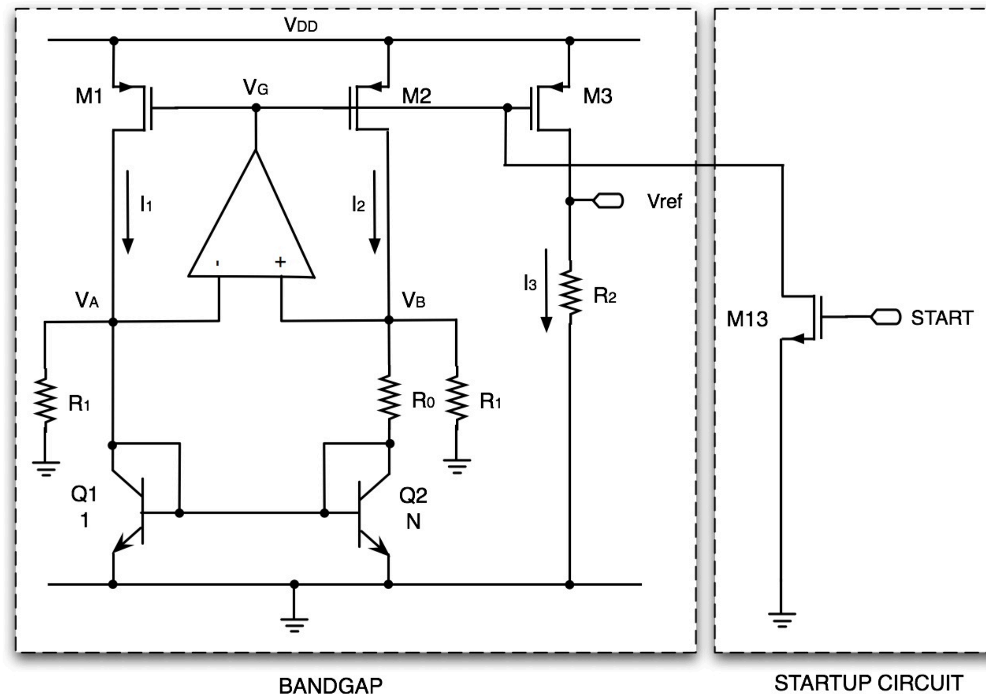
$$\alpha = \frac{R_2}{R_1}$$

- *Assuming no channel length modulation*
- If $V_{REF} \neq V_{DS\text{-}M2}$ => a second op-amp is needed

Startup Circuits

- Bandgap voltage references have two possible operating points => need startup circuits (to avoid $V_A = V_B = 0$)

1. Switch driven by a START signal and temporarily closed at power on, thus forcing the op-amp output at the low potential and causing some current to flow in the arms of the bandgap core
2. During power on, a current start to charge C1, current mirror of M10 charges the gate of M13 and turns M13 on. M13 pulls down the gate of the PMOS current mirror (V_G), injecting current into the bandgap core. After startup, M14 is turned on, then M13 cutoff. When C1 is charged a threshold below the power supply voltage, M10 and M11 are cutoff and the power consumption of the startup is zero after startup. M12 discharges C1 when supply is switched off



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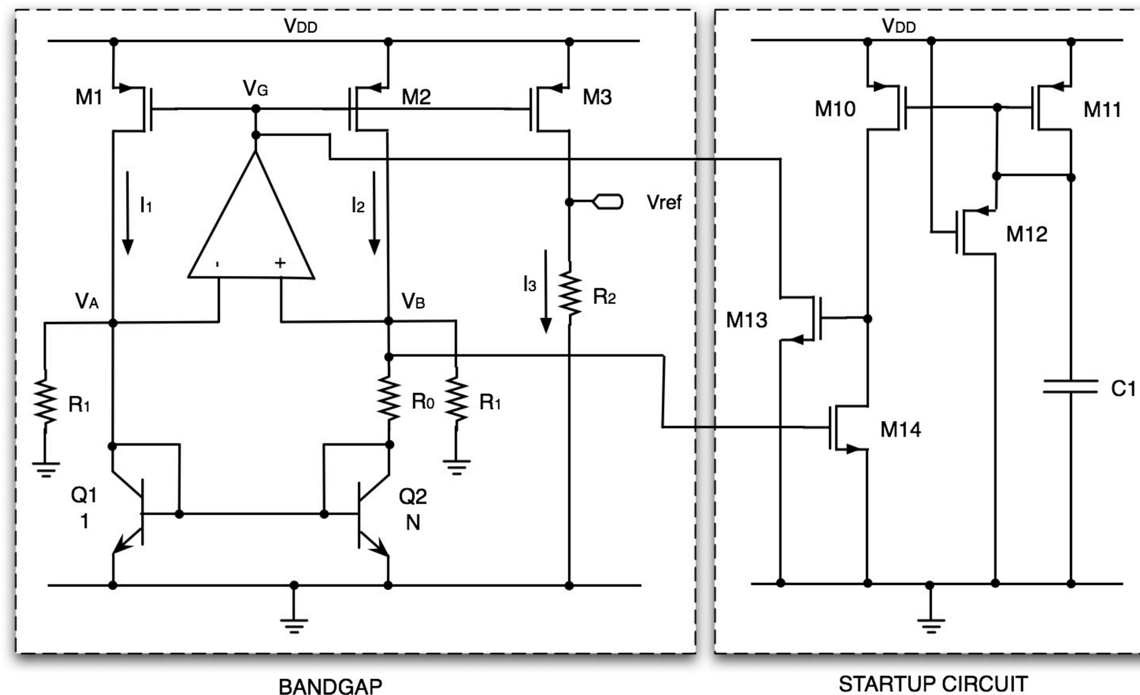
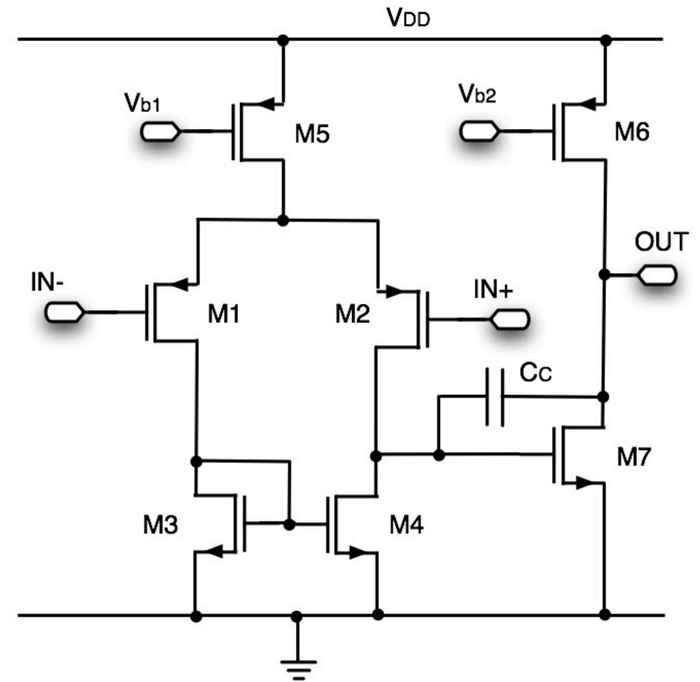
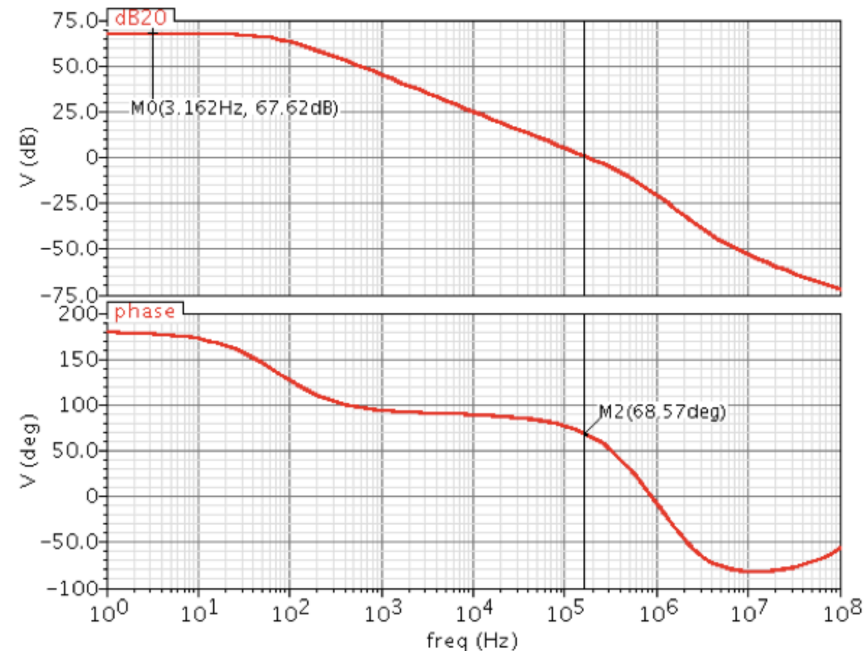


Operational Amplifier

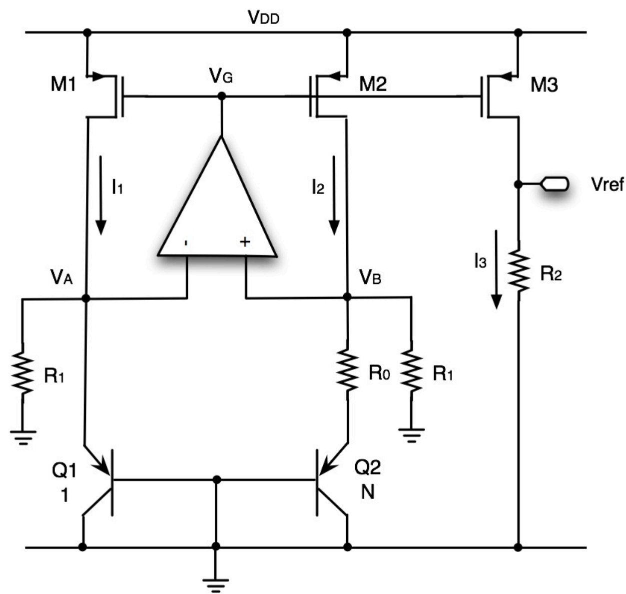
- Architecture: Two-stage Miller OTA
- DC Gain > 60 dB
- GBW > 60 kHz
- Phase Margin: > 60°
- Bias Current: ≈ 1μA
- Compensation capacitance: 1.3 pF

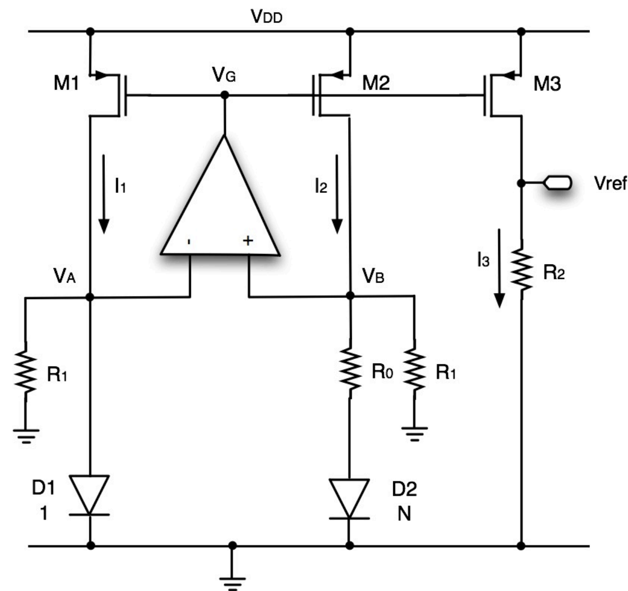


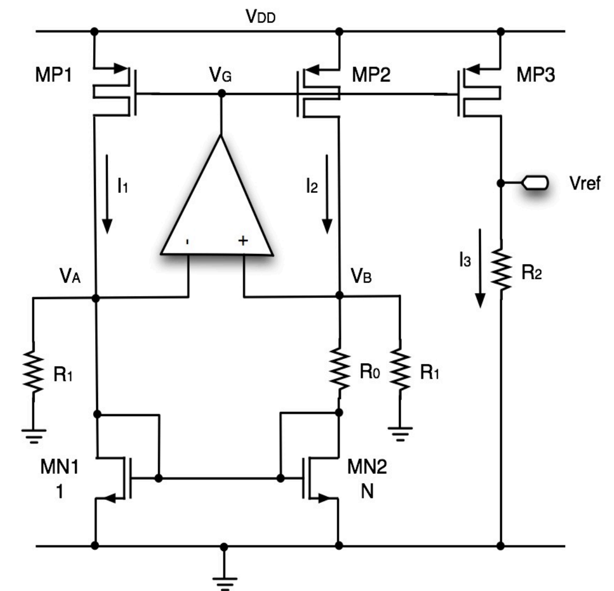


Temp. [°C]	V_{ICM} [mV]	A_{V0} dB	GBW [kHz]	ϕ_0
-50	894	69.8	62	61
0	826	68.4	144	66
27	788	67.6	176	67
50	756	66.9	200	68
100	683	64.9	243	70
150	610	61.5	269	72

Current Mode CM Bandgap References in 65 nm CMOS



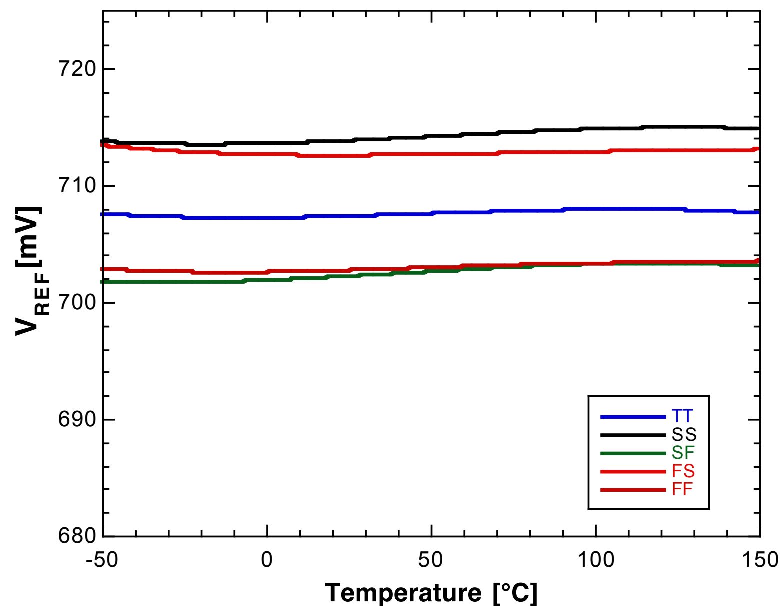




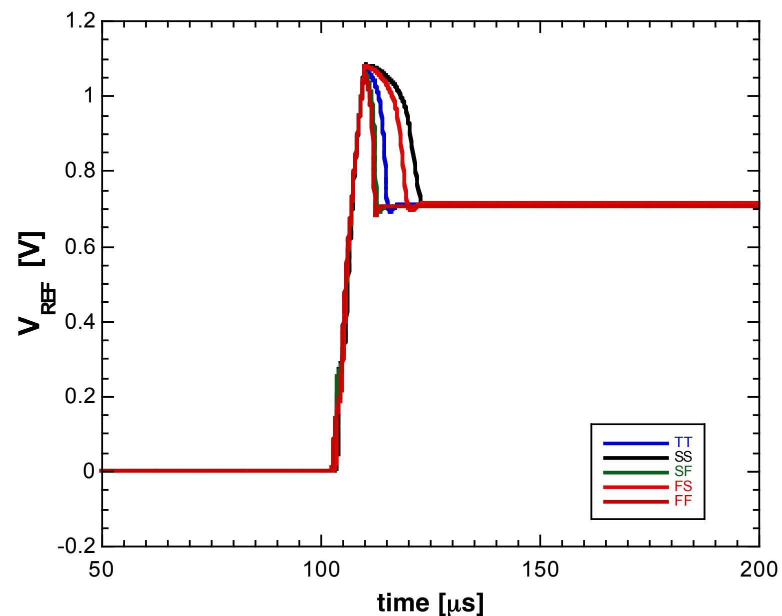
BJT Bandgap Performance

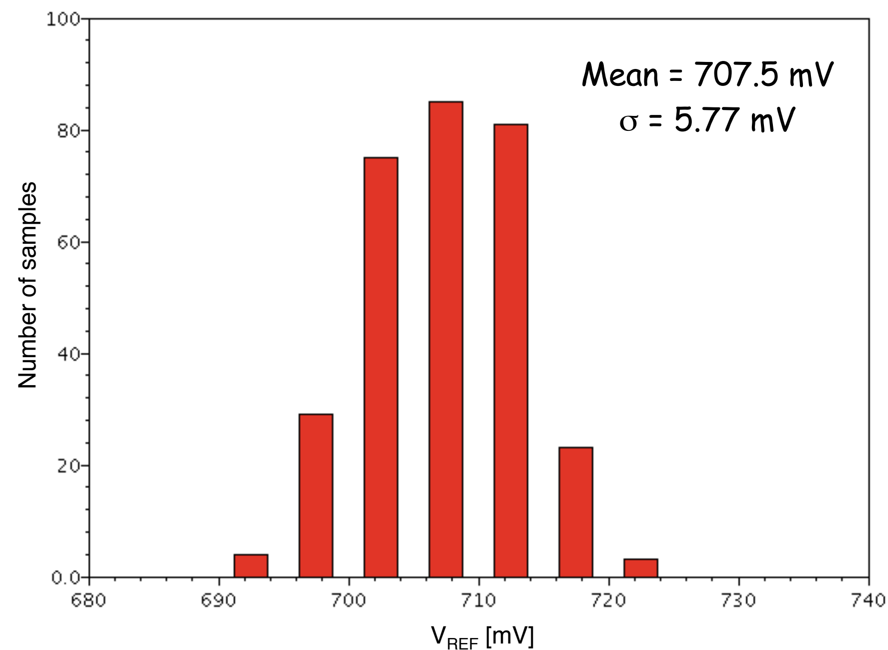
- V_{REF} = 707.5 mV @ 27°C
- Temperature Range: −50°C ÷ 150°C
- V_{REF} variation < 1 mV (ΔV_{Ref} = 0.735 mV)
- Temperature Coefficient = 5.2 ppm/K
- Power Supply = 1.2 V
- Minimum Power Supply = 1.1 V
- Line Regulation ($\Delta V_{REF} / \Delta V_{DD}$) = 0.052
- Power Consumption = 103 μW
- I_2 = 7 μA @ 27°C
- PSR = -28.55 dB @ 1kHz

BJT BGR: Monte Carlo and Four-Corners Simulations



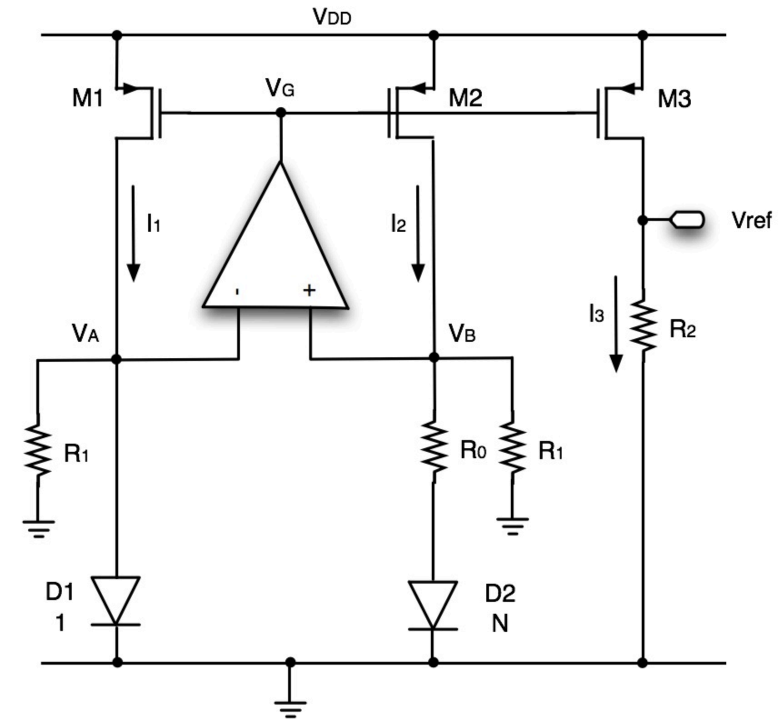
Corner	V_{REF} [mV]	TC [ppm/°C]
FF	702.8	6.93
FS	712.6	5.89
SF	702.2	11.82
SS	713.9	10.16
TT	707.5	5.2

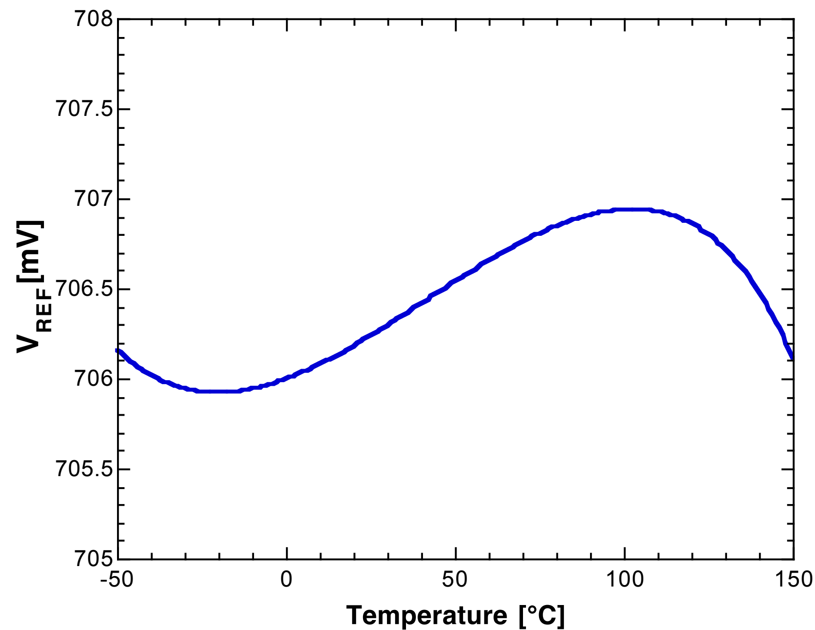




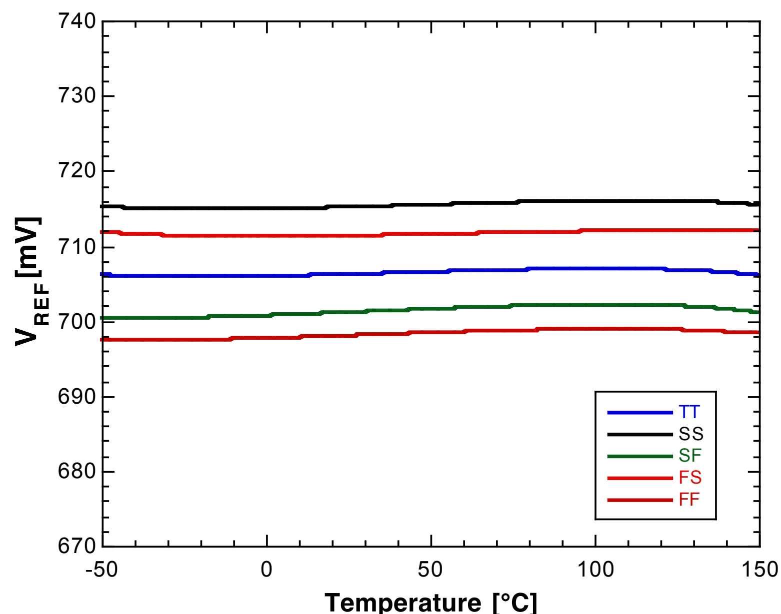
Diode Bandgap Performance

- V_{REF} = 706.3mV @ 27°C
- Temperature Range: –50°C ÷ 150°C
- V_{REF} variation ≈ 1 mV ($\Delta V_{REF-MAX}$ = 1.02 mV)
- Temperature Coefficient = 7.2 ppm/K
- Power Supply = 1.2 V
- Minimum Power Supply = 0.95 V
- Line Regulation (ΔV_{REF} /ΔV_{DD}) = 0.008
- Power Consumption = 103 μW
- I_2 = 14μA @ 27°C
- PSR = -33 dB @ 1kHz

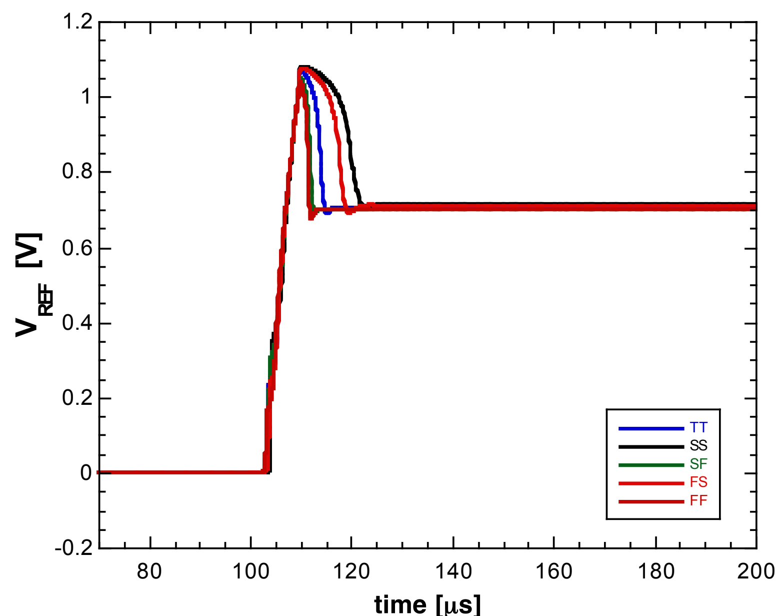


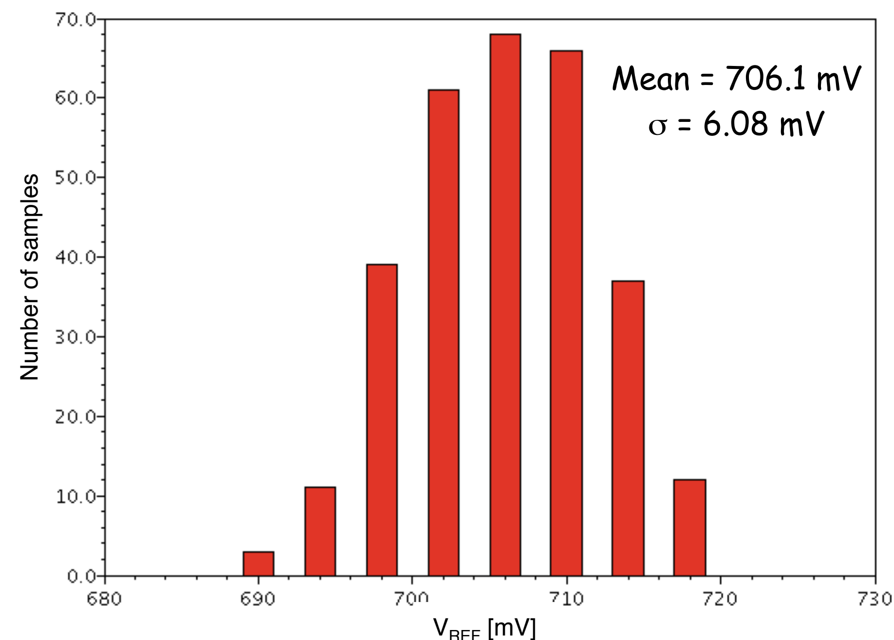


Diode BGR: Monte Carlo and Four-Corners Simulations



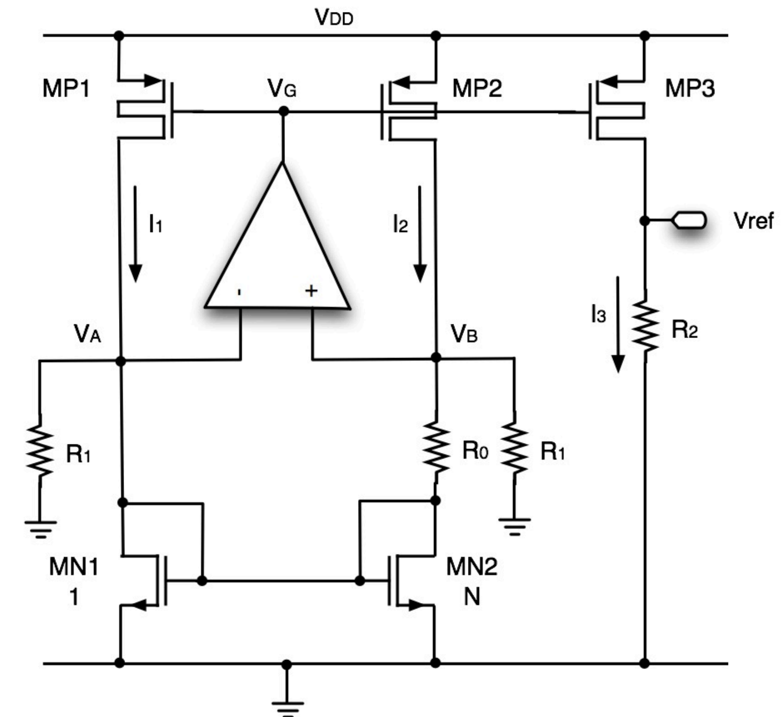
Corner	V_{REF} [mV]	TC [ppm/°C]
FF	698.1	10.3
FS	711.4	5.78
SF	701.2	12.65
SS	715.2	8.16
TT	706.3	7.2

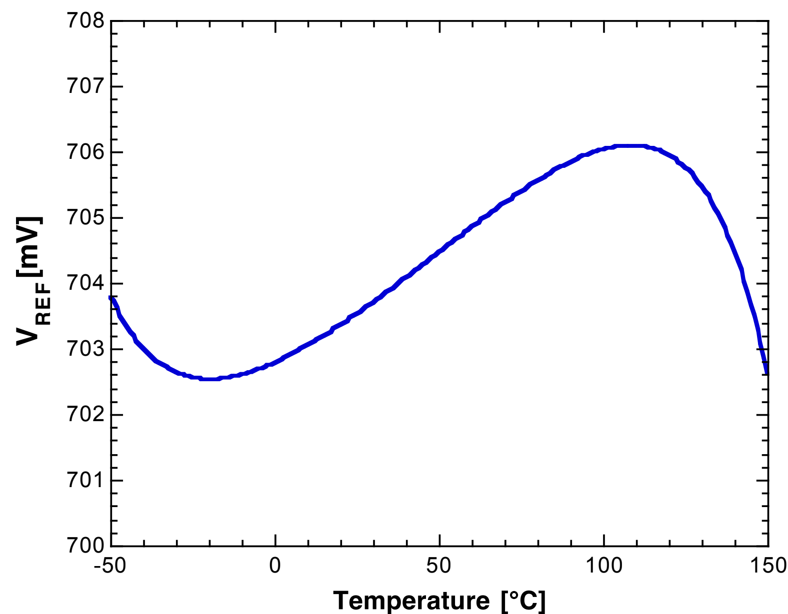




MOS Bandgap Performance

- V_{REF} = 703.6 mV @ 27°C
- Temperature Range: −50°C ÷ 150°C
- V_{REF} variation ≈ 3.5 mV ($\Delta V_{REF\text{-}MAX}$ = 3.55 mV)
- Temperature Coefficient = 25 ppm/K
- Power Supply = 1.2 V
- Minimum Power Supply = 1 V
- Line Regulation ($\Delta V_{REF} / \Delta V_{DD}$) = 0.034
- Power Consumption = 47 μW
- I_{D2} = 6.4 μA @ 27°C
- PSR = -28 dB @ 1kHz
- Inversion Coefficient (I_{C0}) = 0.03 with
  Iz∗ = 0.6 μA, $(W/L)_{M0}$ = 366/1, $(W/L)_{M1}$ = 8x(366/1)



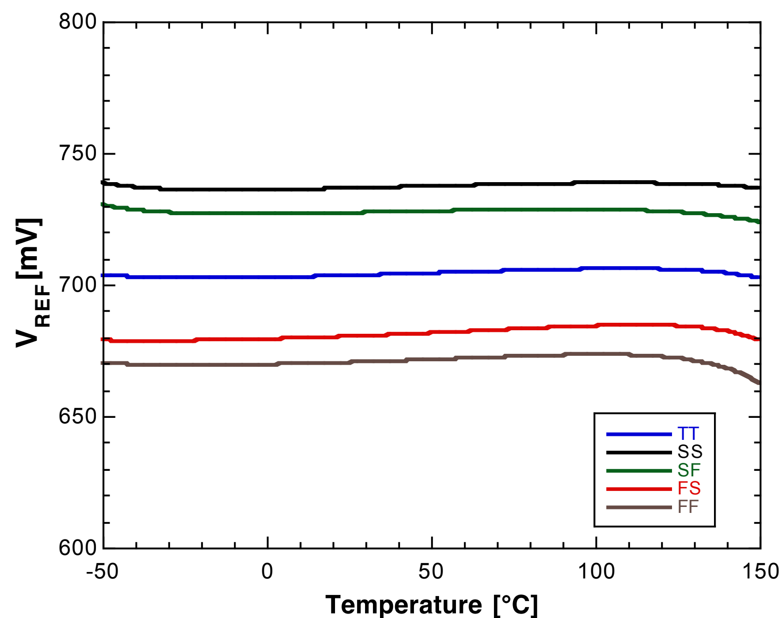


The actual inversion level of a MOS at a given current, can be expressed by means of the Inversion Coefficient $I_{C0}=I_D/(I^*_Z\ W/L)$, which depends on the characteristic normalized drain current I^*_Z ($I^*_Z=2\mu C_{OX} n V_T^2$)

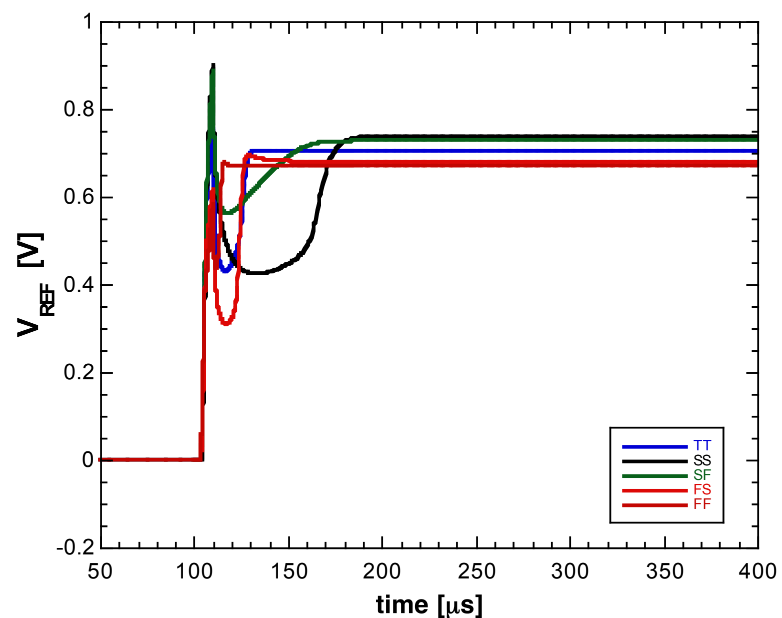
I_{C0} > 10 -> strong inversion region

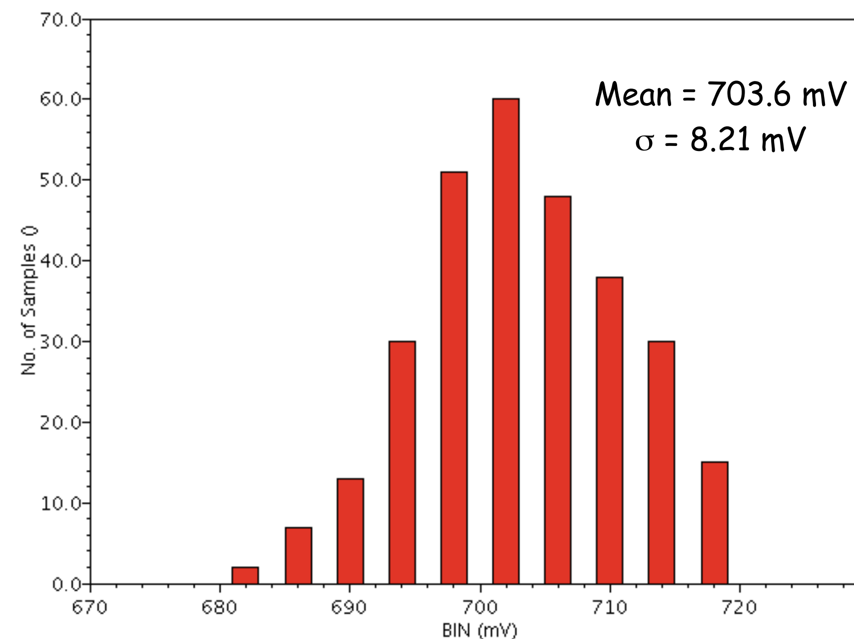
I_{C0} < 0.1 -> weak inversion region

Diode BGR: Monte Carlo and Four-Corners Simulations

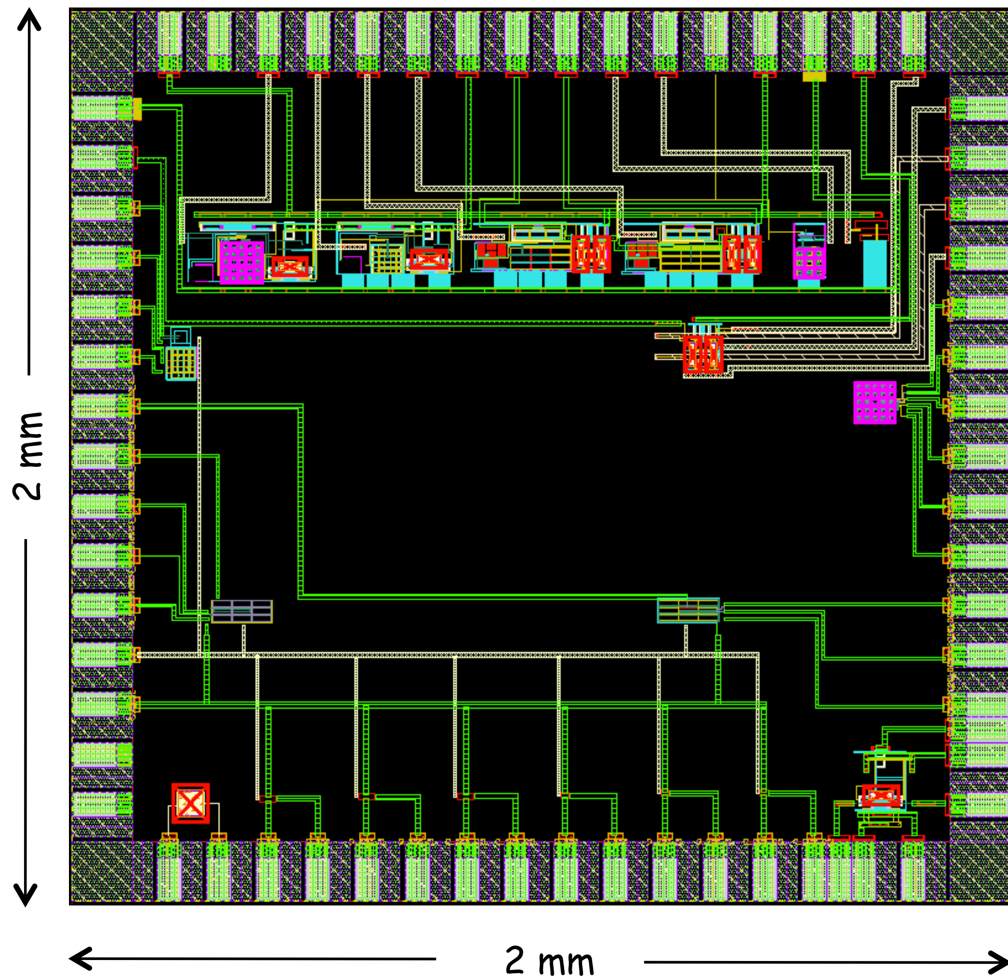


Corner	V_{REF} [mV]	TC [ppm/°C]
FF	670.6	81.56
FS	680.5	43.65
SF	727.4	6.65
SS	736.8	18.43
TT	703.6	25.32

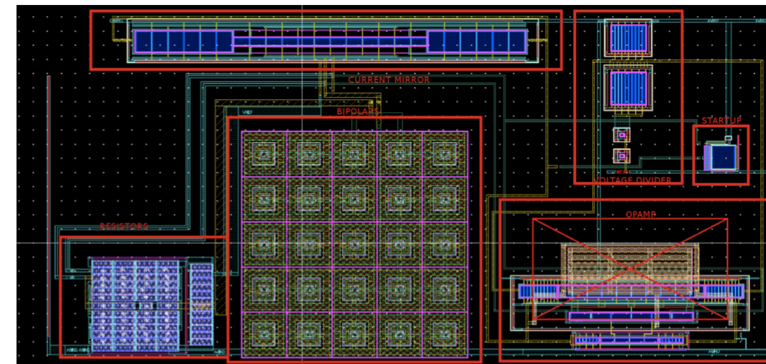




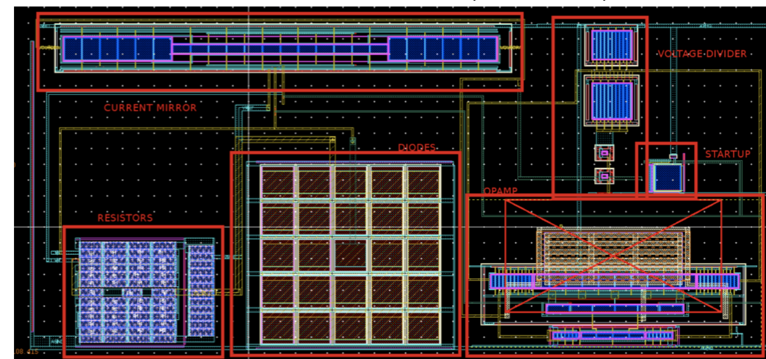
Prototype Chip Layout



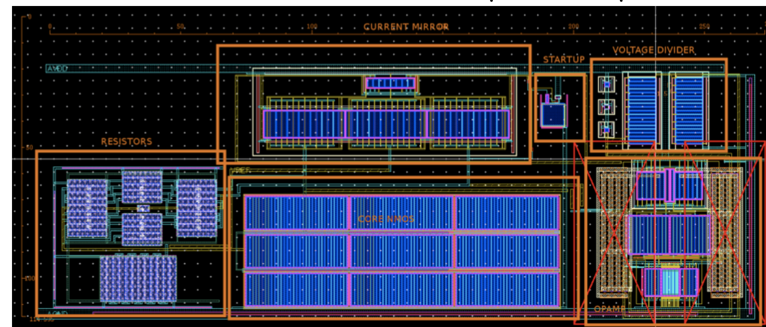
BGR with BJTs 260μm x 120μm



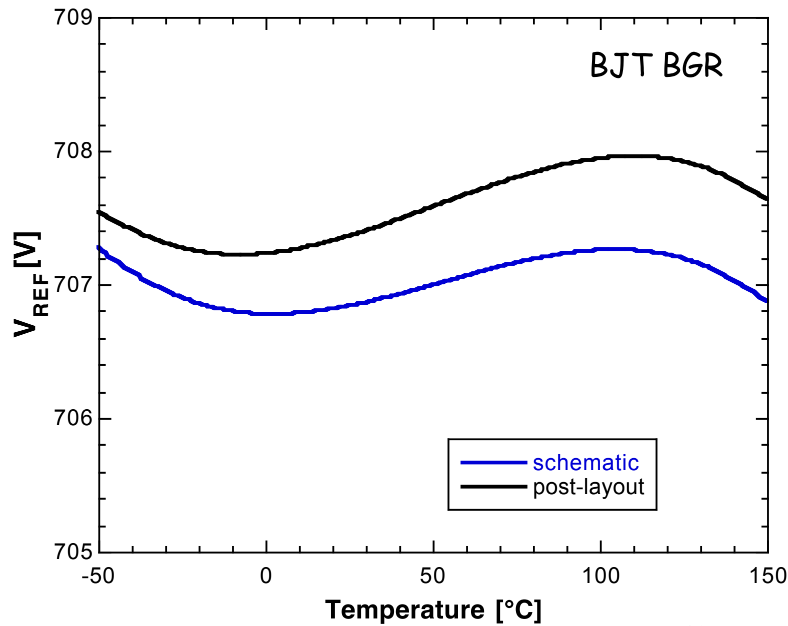
BGR with diodes 240μm x 110μm

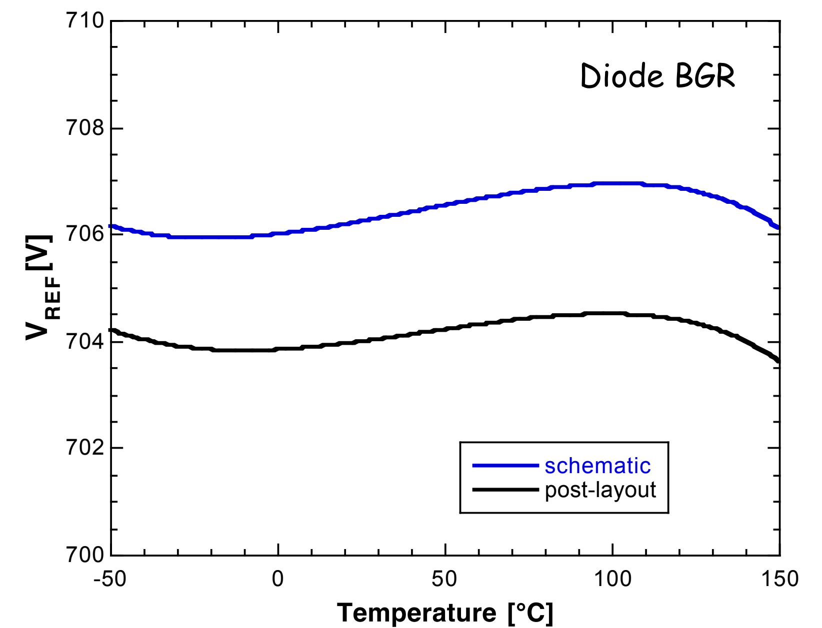


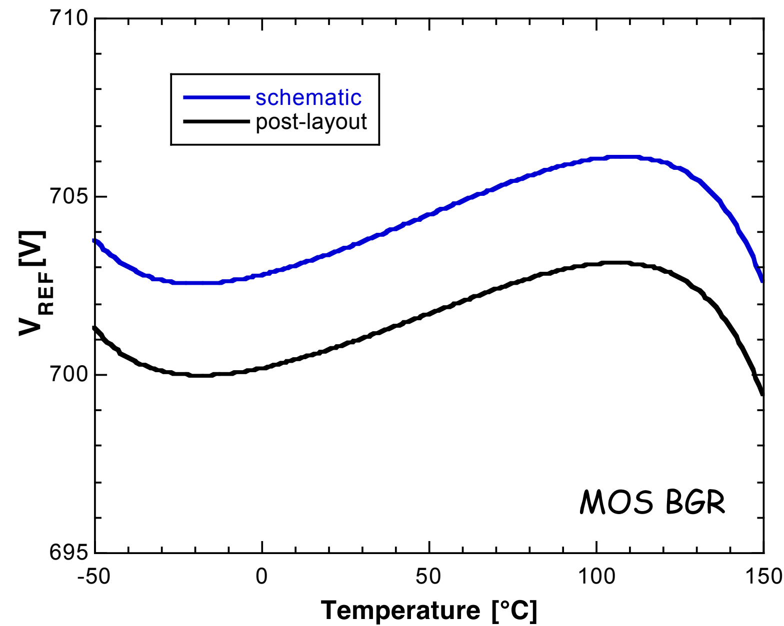
BGR with MOS 240μm x 110μm



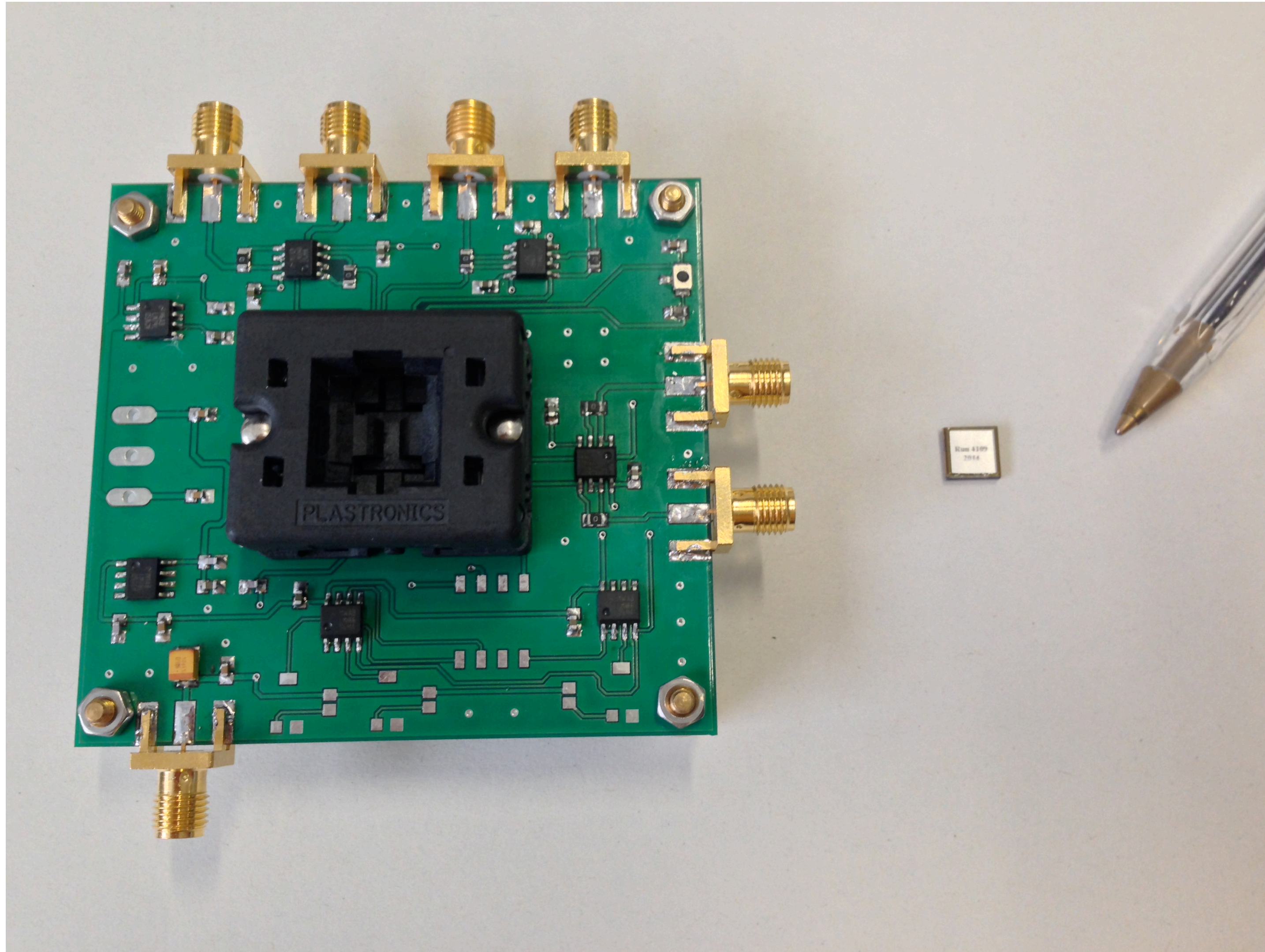
Post-Layout Simulations







Prototype Chip



Conclusions and future activity

- ✓ Three different bandgap reference circuits have been designed and fabricated in the 65nm TSMC CMOS technology
  - ✓ BJT version
  - ✓ Diode version
  - ✓ MOS and MOS with EL versions
- ✓ Prototypes and test board ready -> characterization activity from mid October
- ✓ Irradiation with X-rays machine and neutrons after the test bench characterization

Backup slides

Device characteristic simulations