Design of bandgap reference circuits in a 65 nm CMOS technology for HL-LHC applications

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Topical Workshop on Electronics for Particle Physics (TWEPP 2014)  
22 - 26 September 2014, Aix en Provence, France
Outline

✓ Introduction
✓ Bandgap reference circuit in the 65nm TSMC CMOS technology
  ✓ Bandgap with Bipolar Transistors
  ✓ Bandgap with diodes
  ✓ Bandgap with MOSFETs in weak inversion region
✓ Bandgap components:
  ✓ Startup circuit
  ✓ Operational amplifier
✓ Simulation results
  ✓ Monte Carlo simulation
  ✓ Four-Corner simulation
✓ Prototype chip
✓ Conclusions and future activity
Introduction

- Voltage references are commonly used in a wide range of applications
  - Embedded in complex systems
  - As stand alone devices

- Stability against temperature, power supply and process variations

- Requirements and trade-offs
  - Output voltage precision (Trimming, Curvature compensation vs test time and complexity) -> no trimming
  - Radiation hardness -> (TID effects, displacement damage) -> problems may arise in bipolar transistors and diodes due to charge trapped in oxide above diode and to bulk damage
    - Bandgap circuits with different devices (BJTs, Diodes, MOS, MOS with EL)
  - Power consumption
  - Load current (class A or AB output stage can be included if needed)
  - Layout area
Bandgap References

- Output voltage with a low sensitivity to the temperature: combine a voltage with positive TC with a voltage with negative TC
  - Positive TC (PTAT): thermal voltage \( V_T = kT/q \) (+0.086 mV/K) at 300K
  - Negative TC (CTAT): base-emitter voltage \( V_{BE} \) (-2.2 mV/K) at 300K

- Temperature Coefficient (TC): \( TC = \frac{\Delta V_{OUT}}{V_{OUT} \cdot \Delta T} \)

- Reference Voltage \( V_{REF} = V_{BE} + mV_T \)
  - \( TC \approx 0 \Rightarrow m = 25.6 \Rightarrow V_{REF} \approx 1.2 \text{ V} \) (≈ \( V_{BG} \))

- Voltage mode bandgap circuits: \( V_{REF} = V_{BE} + mV_T \)

- Current mode bandgap circuits: \( V_{REF} = R \left( \frac{V_{BE}}{R_0} + \frac{mV_T}{R_0} \right) = \alpha V_{BG} \)
Voltage Mode (VM) Bandgap References

\[ V_A = V_B = V_{BE\_Q1} \]

\[ \Delta V_{BE} = V_{BE\_Q1} - V_{BE\_Q2} = V_T \ln(N) \]

\[ V_{REF} = V_{BE\_Q1} + \frac{V_T \ln(N)}{R_0} R_1 \]

\[ m = \ln(N) \frac{R_1}{R_0} \]
Current Mode (CM) Bandgap References

- $V_A$ and $V_B$ are kept equal by the op-amp

\[
I_1 = I_2 = \frac{V_T \ln(n)}{R_0} + \frac{V_{BE}}{R_1} = I_3
\]

\[
V_{REF} = V_T \frac{R_2 \ln(n)}{R_0} + V_{BE} \frac{R_2}{R_1}
\]

\[
m = \frac{R_1 \ln(n)}{R_0}
\]

\[
\alpha = \frac{R_2}{R_1}
\]
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$$V_{REF} = V_T \frac{R_2 \ln(n)}{R_0} + V_{BE} \frac{R_2}{R_1}$$

$$m = \frac{R_1 \ln(n)}{R_0}$$

$$\alpha = \frac{R_2}{R_1}$$

- Assuming no channel length modulation
- If $V_{REF} \neq V_{DS-M2}$ => a second op-amp is needed
Bandgap voltage references have two possible operating points => need startup circuits (to avoid $V_A=V_B=0$)

1. Switch driven by a START signal and temporarily closed at power on, thus forcing the op-amp output at the low potential and causing some current to flow in the arms of the bandgap core

2. During power on, a current start to charge $C_1$, current mirror of $M_{10}$ charges the gate of $M_{13}$ and turns $M_{13}$ on. $M_{13}$ pulls down the gate of the PMOS current mirror ($V_G$), injecting current into the bandgap core. After startup, $M_{14}$ is turned on, then $M_{13}$ cutoff. When $C_1$ is charged a threshold below the power supply voltage, $M_{10}$ and $M_{11}$ are cutoff and the power consumption of the startup is zero after startup. $M_{12}$ discharges $C_1$ when supply is switched off.
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Operational Amplifier

- Architecture: Two-stage Miller OTA
- DC Gain > 60 dB
- GBW > 60 kHz
- Phase Margin: > 60°
- Bias Current: ≈ 1 µA
- Compensation capacitance: 1.3 pF

<table>
<thead>
<tr>
<th>Temp. [°C]</th>
<th>$V_{ICM}$ [mV]</th>
<th>$A_{VO}$ dB</th>
<th>GBW [kHz]</th>
<th>$\phi_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>894</td>
<td>69.8</td>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td>0</td>
<td>826</td>
<td>68.4</td>
<td>144</td>
<td>66</td>
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<tr>
<td>27</td>
<td>788</td>
<td>67.6</td>
<td>176</td>
<td>67</td>
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<tr>
<td>50</td>
<td>756</td>
<td>66.9</td>
<td>200</td>
<td>68</td>
</tr>
<tr>
<td>100</td>
<td>683</td>
<td>64.9</td>
<td>243</td>
<td>70</td>
</tr>
<tr>
<td>150</td>
<td>610</td>
<td>61.5</td>
<td>269</td>
<td>72</td>
</tr>
</tbody>
</table>
Current Mode CM Bandgap References in 65 nm CMOS

Topical Workshop on Electronics for Particle Physics (TWEPP 2014), 22 - 26 September 2014, Aix en Provence, France
BJT Bandgap Performance

- $V_{\text{REF}} = 707.5 \text{ mV @ 27°C}$
- Temperature Range: $-50°C \div 150°C$
- $V_{\text{REF}}$ variation $< 1 \text{ mV (}\Delta V_{\text{Ref}} = 0.735 \text{ mV)}$
- Temperature Coefficient = 5.2 ppm/K
- Power Supply = 1.2 V
- Minimum Power Supply = 1.1 V
- Line Regulation ($\Delta V_{\text{REF}} / \Delta V_{\text{DD}}$) = 0.052
- Power Consumption = 103 µW
- $I_2 = 7 \mu\text{A @ 27°C}$
- PSR = -28.55 dB @ 1kHz

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BJT BGR: Monte Carlo and Four-Corners Simulations

Mean = 707.5 mV
$\sigma = 5.77$ mV

<table>
<thead>
<tr>
<th>Corner</th>
<th>$V_{REF}$ [mV]</th>
<th>TC [ppm/°C]</th>
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<tbody>
<tr>
<td>FF</td>
<td>702.8</td>
<td>6.93</td>
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<tr>
<td>FS</td>
<td>712.6</td>
<td>5.89</td>
</tr>
<tr>
<td>SF</td>
<td>702.2</td>
<td>11.82</td>
</tr>
<tr>
<td>SS</td>
<td>713.9</td>
<td>10.16</td>
</tr>
<tr>
<td>TT</td>
<td>707.5</td>
<td>5.2</td>
</tr>
</tbody>
</table>

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Diode Bandgap Performance

- $V_{REF} = 706.3\text{mV} @ 27^\circ\text{C}$
- Temperature Range: $-50^\circ\text{C} \div 150^\circ\text{C}$
- $V_{REF}$ variation $\approx 1 \text{mV}$ ($\Delta V_{REF_{\text{MAX}}} = 1.02 \text{mV}$)
- Temperature Coefficient = 7.2 ppm/K
- Power Supply = 1.2 V
- Minimum Power Supply = 0.95 V
- Line Regulation ($\Delta V_{REF} / \Delta V_{DD}$) = 0.008
- Power Consumption = 103 $\mu$W
- $I_2 = 14\mu\text{A} @ 27^\circ\text{C}$
- PSR = -33 dB @ 1kHz

![Graph showing $V_{REF}$ variation with temperature]

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Diode BGR: Monte Carlo and Four-Corners Simulations

Mean = 706.1 mV
σ = 6.08 mV

<table>
<thead>
<tr>
<th>Corner</th>
<th>( V_{\text{REF}} ) [mV]</th>
<th>TC [ppm/°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>698.1</td>
<td>10.3</td>
</tr>
<tr>
<td>FS</td>
<td>711.4</td>
<td>5.78</td>
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<td>SF</td>
<td>701.2</td>
<td>12.65</td>
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<tr>
<td>SS</td>
<td>715.2</td>
<td>8.16</td>
</tr>
<tr>
<td>TT</td>
<td>706.3</td>
<td>7.2</td>
</tr>
</tbody>
</table>

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MOS Bandgap Performance

- $V_{\text{REF}} = 703.6 \text{ mV} @ 27^\circ\text{C}$
- Temperature Range: $-50^\circ\text{C} \div 150^\circ\text{C}$
- $V_{\text{REF}}$ variation $\approx 3.5 \text{ mV}$ ($\Delta V_{\text{REF-MAX}} = 3.55 \text{ mV}$)
- Temperature Coefficient $= 25 \text{ ppm/K}$
- Power Supply $= 1.2 \text{ V}$
- Minimum Power Supply $= 1 \text{ V}$
- Power Consumption $= 47 \mu\text{W}$
- $V_{\text{REF}}$ variation $\approx 3.5 \text{ mV}$ ($\Delta V_{\text{REF-MAX}} = 3.55 \text{ mV}$)
- Temperature Coefficient $= 25 \text{ ppm/K}$
- $I_{D2} = 6.4 \mu\text{A} @ 27^\circ\text{C}$
- PSR $= -28 \text{ dB} @ 1\text{kHz}$
- Inversion Coefficient ($I_{C0}$) $= 0.03$ with $I_z^* = 0.6 \mu\text{A}$, $(W/L)_{M0} = 366/1$, $(W/L)_{M1} = 8\times(366/1)$

The actual inversion level of a MOS at a given current, can be expressed by means of the Inversion Coefficient $I_{C0} = I_D / (I_z^* W/L)$, which depends on the characteristic normalized drain current $I_z^* (I_z^* = 2\mu C_{\text{ox}} n V_T^2)$

$I_{C0} > 10 \rightarrow$ strong inversion region

$I_{C0} < 0.1 \rightarrow$ weak inversion region
Diode BGR: Monte Carlo and Four-Corners Simulations

Mean = 703.6 mV
\( \sigma = 8.21 \) mV

<table>
<thead>
<tr>
<th>Corner</th>
<th>V_{REF} [mV]</th>
<th>TC [ppm/°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>670.6</td>
<td>81.56</td>
</tr>
<tr>
<td>FS</td>
<td>680.5</td>
<td>43.65</td>
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<tr>
<td>SF</td>
<td>727.4</td>
<td>6.65</td>
</tr>
<tr>
<td>SS</td>
<td>736.8</td>
<td>18.43</td>
</tr>
<tr>
<td>TT</td>
<td>703.6</td>
<td>25.32</td>
</tr>
</tbody>
</table>

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Prototype Chip Layout

BGR with BJTs 260\(\mu\)m x 120\(\mu\)m

BGR with diodes 240\(\mu\)m x 110\(\mu\)m

BGR with MOS 240\(\mu\)m x 110\(\mu\)m

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Post-Layout Simulations

BJT BGR

Diode BGR

MOS BGR

Temperature [°C]

\[ V_{REF} \]
Prototype Chip
Conclusions and future activity

✓ Three different bandgap reference circuits have been designed and fabricated in the 65nm TSMC CMOS technology
  ✓ BJT version
  ✓ Diode version
  ✓ MOS and MOS with EL versions

✓ Prototypes and test board ready -> characterization activity from mid October

✓ Irradiation with X-rays machine and neutrons after the test bench characterization
Backup slides
Device characteristic simulations

BJT

Diode

MOS