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Design of Bandgap Reference Circuits in a 65 nm CMOS Technology for HL-LHC Applications

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This work is concerned with the design and characterization of bandgap reference circuits capable of operating with a power supply of 1.2V in view of applications to HL-LHC experiments. Due to the harsh environment foreseen for these devices, different solutions have been considered and implemented in a 65nm CMOS technology. Together with a conventional structure which exploits bipolar devices, a smaller solution based on diodes and a version with MOS transistors biased in weak inversion region are included. This paper intends to describe and compare the features of the different approaches by means of simulation and experimental results.

Summary

Voltage references, which provide precise, stable and temperature-insensitive DC voltages, are fundamental building blocks in mixed-mode circuits. The bandgap reference (BGR) is one of the most popular voltage reference that successfully achieves these requirements. It generates a voltage, which is obtained from the sum of the voltage across a forward biased pn junction (inversely dependent on the absolute temperature) and a term directly proportional to the absolute temperature (PTAT). Since conventional BGR architectures generate an output voltage of about 1.2 V, in the last few years, new bandgap circuits have been proposed for low-voltage power supply (1.2 V or sub-1 V). This paper discusses a BGR architecture based on a commercial 65 nm CMOS technology and capable of operating with 1.2 V supply. It provides a temperature independent voltage by summing two currents, respectively directly and inversely proportional to the absolute temperature. The proposed IP block has been designed for operation in the harsh radiation environment of the High Luminosity LHC. The 65 nm CMOS technology chosen for this prototype has been tested up to several hundreds of Mrad with promising results, but some components of the BGR, namely bipolar devices, will probably be affected by bulk damage effects. For this reason, in order to understand their behavior after irradiation, three different BGR versions have been designed and submitted for fabrication in a first prototype chip. The first version, which provides the best performance in terms of temperature insensitivity, is based on parasitic PNP bipolar transistors. The second, based on pn diodes, is the best solution in terms of area, while the third one, based on enclosed-layout MOSFETs biased in weak inversion region, is the most promising in terms of radiation tolerance. A copy of the BJT, diode and MOS matrices used in the BGR circuits have been integrated in the test chip to measure the static and signal characteristics of the devices after irradiation. The full discussion of the bandgap reference circuits together with preliminary radiation hardness tests will be provided in the conference paper.

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