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The Readout Chain for the PANDA MVD Strip Detector

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The PANDA experiment at the future FAIR facility will study annihilation reactions of antiprotons on stationary targets. The Micro-Vertex-Detector (MVD) as part of the tracking system will permit precise tracking and detection of secondary vertices. It is made of silicon pixel detectors and double-sided silicon strip detectors.
Developments for the readout of the strip detectors, ranging from a customized self-triggering readout ASIC and a Module Data Concentrator ASIC at the stave level over the GigaBit Transceiver (GBT) link to the FPGA-based off-detector electronics, will be presented.
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Summary

The future international accelerator facility FAIR (Facility for Antiproton and Ion Research) will host multiple experiments. A focus will be on experiments with antiprotons. The PANDA (antiProton ANnihilation at DArmstadt) experiment will study the strong interaction in annihilation reactions between an antiproton beam and a stationary gas target.
The PANDA detector, composed of a target- and forward spectrometer to nearly cover the full solid angle, consists of different sub-detectors for tracking, particle identification and calorimetry. The Micro-Vertex-Detector (MVD) as the innermost part of the tracking system will facilitate precise tracking and detection of secondary vertices. The MVD will comprise four barrels of silicon detectors, two layers consisting of silicon pixel sensors, and two layers of double-sided silicon strip sensors as well as a set of forward disks employing both technologies.
The strip part will contain approximately 200,000 channels that need to be read out using a highly integrated front-end chip. Since the unique data acquisition concept of the PANDA detector demands that every sub-detector is able to detect hits without requiring an external trigger, a custom-made ASIC is being developed. This self-triggering PASTA (PAnda STrip Asic) chip will employ the Time over Threshold (ToT) technique to digitize the hit amplitude and utilize time-to-digital converters (TDC) with analog interpolators to provide a high-precision time stamp of the hit.
A custom-made Module Data Concentrator ASIC (MDC) will multiplex the data of all front-ends of one double-sided strip detector towards the CERN-developed GBT link chip (GigaBit Transceiver). The MDC will be able to perform feature extraction algorithms to reduce the amount of data to be send off the detector. The µTCA based MVD Multiplexer Board (MMB) at the off-detector site will receive and concentrate the data from the GBT links and transfer it to FPGA-based compute nodes for global event building that combines all sub-detectors.
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