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Demonstrator System for the Phase-I Upgrade of the Trigger Readout Electronics of the ATLAS Liquid-Argon Calorimeters

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The trigger readout electronics of the ATLAS LAr Calorimeters will be improved for the Phase-I luminosity upgrade of the LHC to enhance the trigger feature extraction. Signals with higher spatial granularity will be digitized and processed by newly developed front-end and back-end components. In order to evaluate technical and performance aspects, a demonstrator system is being set up which is planned to be installed on the ATLAS detector during the upcoming LHC run. Results from system tests of the analog signal treatment, the trigger digitizer, the optical signal transmission and the FPGA-based back-end are reported.

Summary

The installation of the upgraded trigger readout of the ATLAS Liquid Argon (LAr) calorimeters is foreseen in the LHC shut-down period of 2018-2019 in order to prepare for the LHC Phase-I luminosity upgrade. The improved read-out of the trigger signals will process 34000 so-called Super-Cells at every LHC bunch-crossing at a frequency of 40 MHz. Energy sums in each calorimeter layer will be provided in a spatial granularity much finer than in the current ATLAS trigger system. This will allow a real-time extraction of trigger features using algorithms inspired by offline data processing. In the first stage of signal processing, the Super-Cell energy deposits need to be calculated at the correct bunch-crossing while efficiently suppressing out-of-time pile-up. This requires a combined optimization of analog signal shaping, signal digitization and digital signal processing.

In order to perform detailed technical and performance tests of the complete system, a demonstrator set-up is foreseen to be implemented already in current LHC shut-down period. One Front-End Crate (FEC) covering a region of $\Delta\eta \times \Delta\phi = 1.4 \times 0.4$ of one LAr half-barrel will be equipped with prototype components. The demonstrator system will already provide the full functionality of the future LAr Phase-I trigger system. It is composed of a new FEC baseplane, new Layer Sum Boards mounted on the existing front-end boards, a prototype LAr Trigger Digitizer Board (LTDB), additional signal fibers, and a prototype of the LAr Digital Processing Board (LDPB).

One LTDB will be able to digitize up to 320 Super-Cell channels with 12-bit ADCs. Data are transmitted on a multi-ribbon optical link at a speed of 5.44 Gbps per fiber. Two prototype versions are currently being evaluated with a digital mother board and analog mezzanine cards, or vice-versa. The prototype implements 40 commercial TI ADS5272 ADCs qualified to be sufficiently radiation tolerant. Moreover, two custom ADC developments based on SAR and pipeline techniques in 130nm CMOS technology are under development. The data preparation and transmission by the LTDB prototype is performed by Xilinx Kintex-7 FPGAs.

The current LDPB back-end prototype implements data reception and processing on an ATCA board with three ALTERA Stratix-V FPGAs, including a custom protocol interface to the front-end and a 10-Gbps Ethernet interface to the PC controller and data storage. The next generation prototypes are planned to employ Xilinx Virtex-7 and ALTERA Arria-10 devices mounted on Advance Mezzanine Cards (AMC) for further comparison of their performance and their resource utilization.

Currently, the demonstrator system is being operated in an off-detector installation where analog signals similar to the real detector pulses can be injected. Results from the performance of the different prototype

components and their interplay will be reported, including analog signal parameters, like noise and cross-talk, as well as digital signal treatment, fast data transmission, and integration into the ATLAS over-all trigger and control system.

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