Low-Power Clock Distribution Circuits for the Macro Pixel ASIC

L. Gaioni[1], F. De Canio[2,3], M. Manghisoni[1,3], L. Ratti[2,3], V. Re[1,3], G. Traversi[1,3], A. Marchioro[4], K. Kloukinas[4]

[1] University of Bergamo, Department of Engineering, Dalmine (BG), Italy

[2] University of Pavia, Department of Electrical, Computer and Biomedical Engineering, Pavia, Italy

[3] INFN Sezione di Pavia, Pavia, Italy

[4] CERN European Organization for Nuclear Research, Geneva, Switzerland

Introduction

The innermost part of the **CMS tracker** at the HL-LHC is based on a combination of pixelated and short strip sensors, the so-called **Pixel-Strip** (PS)**module**. The short strip layer is read out as a classical strip detector by means of the Strip Sensor ASIC (SSA), while the pixelated layer is readout by means of the **Macro Pixel ASIC** (MPA), bump bonded to the sensor, as normally done in hybrid pixels. **Clock distribution** circuits account for a significant fraction of the **power dissipation** in the readout chip: the clock signal must indeed be distributed all over the chip with minimum possible skew. While keeping the skew at a minimum, clock distribution networks waste a significant amount of power.

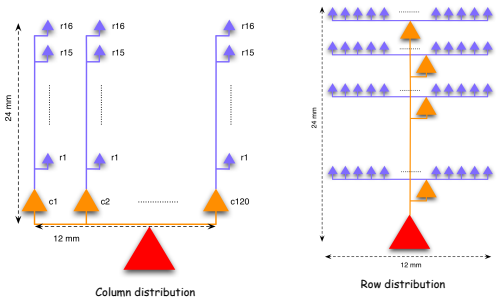
This work reviews different CMOS circuit architectures envisioned for **low power clock distribution** in the MPA. Two main topologies will be discussed, one based on standard supply voltage, the other on auxiliary, reduced supply. Circuit performance, in terms of power consumption and speed, is evaluated for each of the proposed solutions and compared with that relevant to standard CMOS drivers.

The Macro Pixel ASIC

MPA main characteristics

- 16x120 matrix featuring a pixel size of 1500 µm x 100 µm
- Designed in a 65 nm CMOS technology
- Limited power budget (~200 mW) available to carry out the complex functions integrated in the chip
- **40 MHz** clock operating frequency

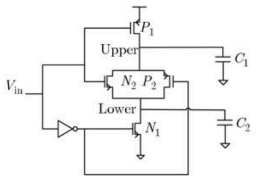
Two routing schemes for the clock distribution have been investigated: the **column distribution** (CD) and the **row distribution** (RD)



Low Power Architectures

- Review and comparison of different architectures already published in the literature
- Simulations of buffers able to reduce the clock swing to a predetermined value
- Each architecture evaluated in terms of **power** and **propagation delay**
- Possible benefits evaluated by a comparison with conventional full swing (FS) buffers, supplied with 1.2 V
- The simulated structures include a clock driver distributing a 40 MHz clock signal to 16 receivers through a clock line featuring a lumped parasitic capacitance equal to 5 pF (this emulate one column in the CD scheme of the MPA)

Charge redistribution

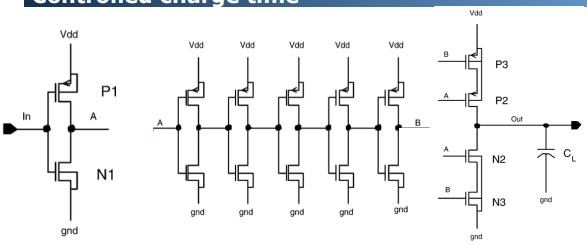


- Vin *low*: $C_1 \rightarrow V_{DD}$ and $C_2 \rightarrow$ gnd
- Vin *high*: P1 and N1 are off, the transmission gate is on and the charge is redistributed between C1 and C2

$$V_{upper} = V_{lower} = \frac{C_1 \cdot V_{DD}}{C_1 + C_2}$$

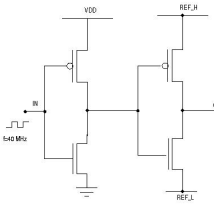
- Analog receiver: CMOS differential stage with active load followed by two inverters
- **Delay**: 935 ps (FS buffer 975 ps)
- **Power** of the driver: 30 µW (FS buffer 290 µW)

Controlled charge time



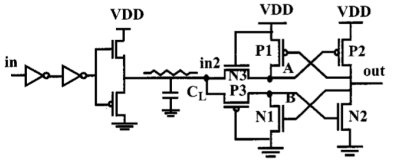
- Output swing controlled by chain (A→B) delay, V_{th} of MOSFETs, W of the output stage, bus capacitance C_L
- $V_{OUT\_L} < V_{th,N}$ and $V_{OUT\_H} > V_{DD} - |V_{th,P}|$
- The power consumption is about: $f\ C_L\ V_{DD}\ V_{SW}$ (where $V_{SW} = V_{OUT\_H} - V_{OUT\_L}$)
- **Delay**: 960 ps (FS buffer 975 ps)
- **Power** of the driver: 92 µW (FS buffer 290 µW)
- A cascade of two inverters can be used for full swing signal recovery

Drivers with two extra supplies



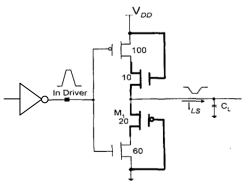
- Two inverter driver: the second one uses two extra reference voltages (REF_H, REF_L) and LVT MOSFETs
- A cascade of two inverters can be used as a receiver, but a differential amplifier can be implemented (if needed)
- **Delay**: 965 ps (FS buffer 975 ps)
- **Power** of the driver: 37 µW (FS buffer 290 µW)
- Strong reduction of the power dissipated with same delay
- Main issue is to generate (low power) REF_L and REF_H

Static source follower



- The driver limits the interconnect swing from $|V_{th,P}|$ to V_{DD}-$V_{t,N}$
- The receiver is composed of a transmission gate and a cross-coupled latch circuit
- Transistors P1 and N1 provide positive feedback to completely cut off P2 and N2
- **Delay**: 700 ps (FS buffer 975 ps)
- **Power** of the driver: 123 µW (FS buffer 290 µW)

Static Reduced-Swing

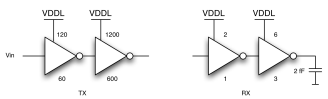


- This scheme reduces the swing of the driver between $V_{th,P}$ and (V_{DD}-$V_{th,N}$)
- Poor rise and fall time
- **Delay**: 1150 ps (FS buffer 975 ps)
- **Power** of the driver: 110 µW (FS buffer 290 µW)

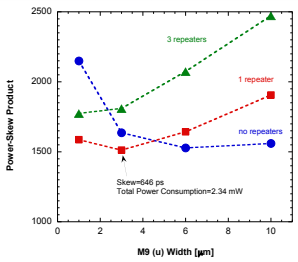
Clock distribution architectures for the MPA

- **CD scheme** for the MPA would consume a huge amount of power due to the large number of columns
- The proposed solution features an **RD architecture** where a central buffer column distributes the clock along the matrix and 1 clock line per row distributes the clock to the 120 pixel cells in the row
- A study of the optimum number and dimension of repeaters to be placed on the central column (laid out with ultrathick metal M9) has been carried out
- Two possible implementations have been investigated, based on CMOS buffers supplied with **reduced VDD** and on **low swing** drive
- Such solutions are modified versions of the schemes shown in the previous section, and have been chosen taking also into account circuit reliability
- We evaluated each architecture in terms of **total power consumption** (including the contribution from receivers and repeaters) and the maximum **skew** between pixels. A comparison with conventional full swing buffers (1.2 V) has been carried out.

Reduced supply voltage



Standard CMOS buffers as TXs and RXs, supplied by VDDL=800 mV



	Skew @ rising edge [ps]	Skew @ falling edge [ps]	Average Skew [ps]	Total Power Consumption [mW]	Power-Skew Product [fJ]
0.8V Solution	632	660	646	2.34	1512
Low-swing	489	636	562	4.34	2441
1.2V Solution	435	447	441	5.41	2386

Low swing driver

The M3 nMOS transistor is inserted between the pMOS and nMOS transistors of a simple inverter to decrease the output voltage swing. An asymmetric inverter involving an LVT nMOS and a HVT pMOS can be used as the receiver.