Contribution ID: **86** Type: **Poster**

Low-Power Clock Distribution Circuits for the Macro Pixel ASIC

Wednesday, 24 September 2014 16:57 (1 minute)

Clock distribution circuits account for a significant fraction of the power dissipation of the Macro Pixel ASIC (MPA), designed for the pixel layer readout of the so-called Pixel-Strip module in the innermost part of the CMS tracker at HL-LHC. This work reviews different CMOS circuit architectures envisioned for low power clock distribution in the MPA. Two main topologies will be discussed, based on standard supply voltage and on auxiliary, reduced supply. Circuit performance, in terms of power consumption and speed, is evaluated for each of the proposed solutions and compared with that relevant to standard CMOS drivers.

Summary

The innermost part of the CMS tracker at the HL-LHC is based on the combination of pixelated and short strip sensors, the so-called Pixel-Strip module (PS). The short strip layer is read out as a classical strip detector by means of the Strip Sensor ASIC (SSA), while the pixelated layer is read out by means of the Macro Pixel ASIC (MPA), bump bonded to the sensor, as normally done in hybrid pixels. The MPA consists of a matrix of 16x128 pixels of dimension 1500 μm x 100 μm, and will be designed in a 65 nm CMOS technology. Based on an estimation deriving from a detailed circuit study for the CERN NA62 Giga-Tracker, where a comparable pixel area is used, a power budget of 80 μW per pixel channel is assumed. Clock distribution circuits account for a significant fraction of the power dissipation in the readout chip: the clock signal must indeed be distributed all over the chip with minimum possible skew. While keeping the skew at a minimum, clock distribution networks waste a significant amount of power. Several methods have been proposed in the literature to reduce power consumption. Such methods mainly deal with the reduction of the dynamic component of the total power dissipation, obtained by reducing the voltage swing of the clock signal or by reducing the supply voltage V_{DD}. In the first case, a linear reduction in the power dissipation can be achieved, whereas in the second one a quadratic reduction can be obtained if the clock signal amplitude is scaled by the same factor as V_{DD}. This work reviews different low power, CMOS circuit architectures and presents a thorough analysis of their effectiveness and limitations. In particular, two main circuit topologies are discussed, based on standard supply voltage and on auxiliary, reduced supply respectively. Circuits of the first topology include source follower buffers, static reduced swing drivers and low swing drivers based on charge redistribution, just to name a few. Circuits of the second topology achieve the reduced power consumption by means of a separate reduced supply voltage, which can be generated on chip.The conference paper will discuss the performance of each architecture in terms of power consumption and speed. The power-delay product will be used as a figure of merit for each circuit. The possible benefits associated with such architectures will be evaluated by a comparison with conventional, full swing CMOS buffers.

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Session Classification: Second Poster Session

Track Classification: ASICs