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The FC7 AMC for Generic DAQ/Control Applications in CMS

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The FC7 is a flexible, μ TCA compatible Advanced Mezzanine Card (AMC) for generic data acquisition/control applications. Built around the Xilinx Kintex 7 FPGA, the FC7 provides developers with a platform which has access to a large array of configurable I/O, primarily delivered from onboard FPGA Mezzanine Card (FMC) headers. Targeting users of high speed optical links in high energy physics experiments, the board is capable of driving and receiving links up to 10Gb/s. This paper presents test results from the first set of pre-production prototypes and reports on FC7 uses and applications towards upgrades in CMS.

Summary

The FC7 is a flexible, μ TCA compatible Advanced Mezzanine Card (AMC) for generic data acquisition/control applications. An evolution of existing board designs, the FC7 development is a collaborative effort between CERN and Imperial College London.

Built around the Xilinx Kintex 7 FPGA, the FC7 provides developers with a platform which has access to a large array of configurable I/O, primarily delivered from onboard FPGA Mezzanine Card (FMC) headers. The FC7 can support up to two FMC mezzanines, providing up to 136 lines (configurable as either single-ended or differential) for user-defined purposes. The maximum specified data rate for these configurable lines is 710 Mb/s (1.25 Gb/s Double Data Rate) differential. Additionally targeting users of high speed optical links in high energy physics experiments, the FC7 is capable of driving and receiving serial links up to 10Gb/s. Through the use of appropriate FMCs, a maximum bandwidth of 200Gb/s is available via the serial links over the front panel.

Designed as a full height, double width AMC, the FC7 is suitable for μ TCA-based scalable production or test systems, as well as for bench-top prototyping. In a crate (or using a custom AMC extender), the board can communicate with the outside world through the two standard Gigabit Ethernet endpoints. The FC7 also supports quad-lane PCI Express (PCIe 2.0) and provides an additional 6 high speed serial links over the backplane for communication, depending on its configuration, with the outside world or with other cards in the crate. The FC7 is able to support a range of multi-gigabit serial protocols both over the backplane as well as the front panel FMCs by means of a configurable clock distribution tree. This includes standard (e.g. 10Gigabit Ethernet, SATA, SRIO) and custom protocols (e.g. LHC clock synchronous protocols) such as the CERN Gigabit Transceiver (GBT). In addition to the PICMG standards, the board has been designed to be compatible with CMS applications, where some of the backplane ports have non-standard implementations.

A firmware ecosystem has been developed for the FC7 which wraps the details of the board functionality in order to provide developers with a simple entry point around which user-specific firmware can be integrated. A communication path to the register space is provided by IPBus allowing full control of the board, from clock configuration, to accessing the 4Gb external DDR3 RAM, to loading and booting from a repository of firmware images on an external uSD card.

This paper presents test results from the first 15 pre-production prototypes, submitted to two different manufacturers and delivered in January 2014, and reports on the uses and applications of the FC7 towards various upgrades in CMS.

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