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The Clock and Control System for the EuXFEL 2D Detectors: Firmware and System Integration

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The firmware structure and system integration of the final Clock and Control (CC) hardware for the EuXFEL 2D mega-pixel detectors are presented. The hardware was developed as a combination of an AMC board and a custom RTM that would work in a MTCA.4 crate. The firmware consists of a number of modules interconnected around a bus/register system that communicates to the control system over PCIe. The firmware also communicates with the front end electronics, veto unit and the timing system. The control of the system operation is through a device implemented on the EuXFEL DAQ software framework.

Summary

The final Clock and Control (CC) system for the EuXFEL 2D megapixel detectors based on the MTCA4 technology consists of an AMC board and an RTM. The development of the hardware part was described in earlier papers. This paper describes the firmware structure and integration into the EuXFEL software framework.

The firmware for the CC system is made up of customised reusable modules centred around a bus/register structure called IIBus and it appears in the application part of the overall DAMC2 firmware. The main components include the modules for communication with the Timing Receiver (TR) board, the Veto Unit (VU), the detector Front-End Modules (FEMs), and the crate CPU board. These modules are designed as general purpose drop-in parts that can be customised through the use of generics. The TR communication involves a source-synchronous serial data link at 108 MHz through two MLVDS channels on the MTCA4 backplane which transmits beam related information. The trigger is a pulse on another channel. The VU communication is through a 2.5 Gbps serial link realised on a fibre cable connected to the SFPs on the front panel of the DAMC2 board (one SFP for each VU link). The FEM communication comprises 2 source-synchronous serial links (FAST data and veto) with a 99 MHz clock transmitted as LVDS pairs on a CAT5e Ethernet cable. CPU board communication is a PCIe link through the MTCA4 backplane.

The firmware modules communicate with each other through the registers of the IIBus and the FIFOs that are generated as a part of the main control module of the firmware. Additionally, for test purposes there are modules that emulate the functionality of the actual modules such as generating triggers and the train ID information.

The CC system integrates to the overall DAQ system through the EuXFEL software framework, Karabo. Karabo sees the CC system as a device which is a controllable object with a state machine based program flow having its own graphical user interface. The control of the device is done through accessing the CC registers. The register structure consists of the control and the status parts. The control registers can modify every aspects of the hardware such as switching the FEM clock between various sources and changing its frequency, switching between the master and the slave mode of operation, and selecting between the normal and the various standalone operation modes that enables the controller to test and simulate each communication module in the firmware.

The integration of the CC system to the EuXFEL software framework has been accomplished seamlessly and the tests are being carried out for integration to the other parts of the EuXFEL system both at UCL and the other detector groups. The results so far show a correct operation in communicating with the various subsystems and the way the data is shared between the different modules in the firmware. The next step is to set up a slice test involving all possible components of the data acquisition chain.

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