A TTC upgrade proposal using bidirectional 10G-PON FTTH technology

Topical Workshop on Electronics for Particle Physics
Aix En Provence 24/09/2014

Dimitrios-Marios Kolotouros
Sophie Baron, Csaba Soos and Francois Vasey

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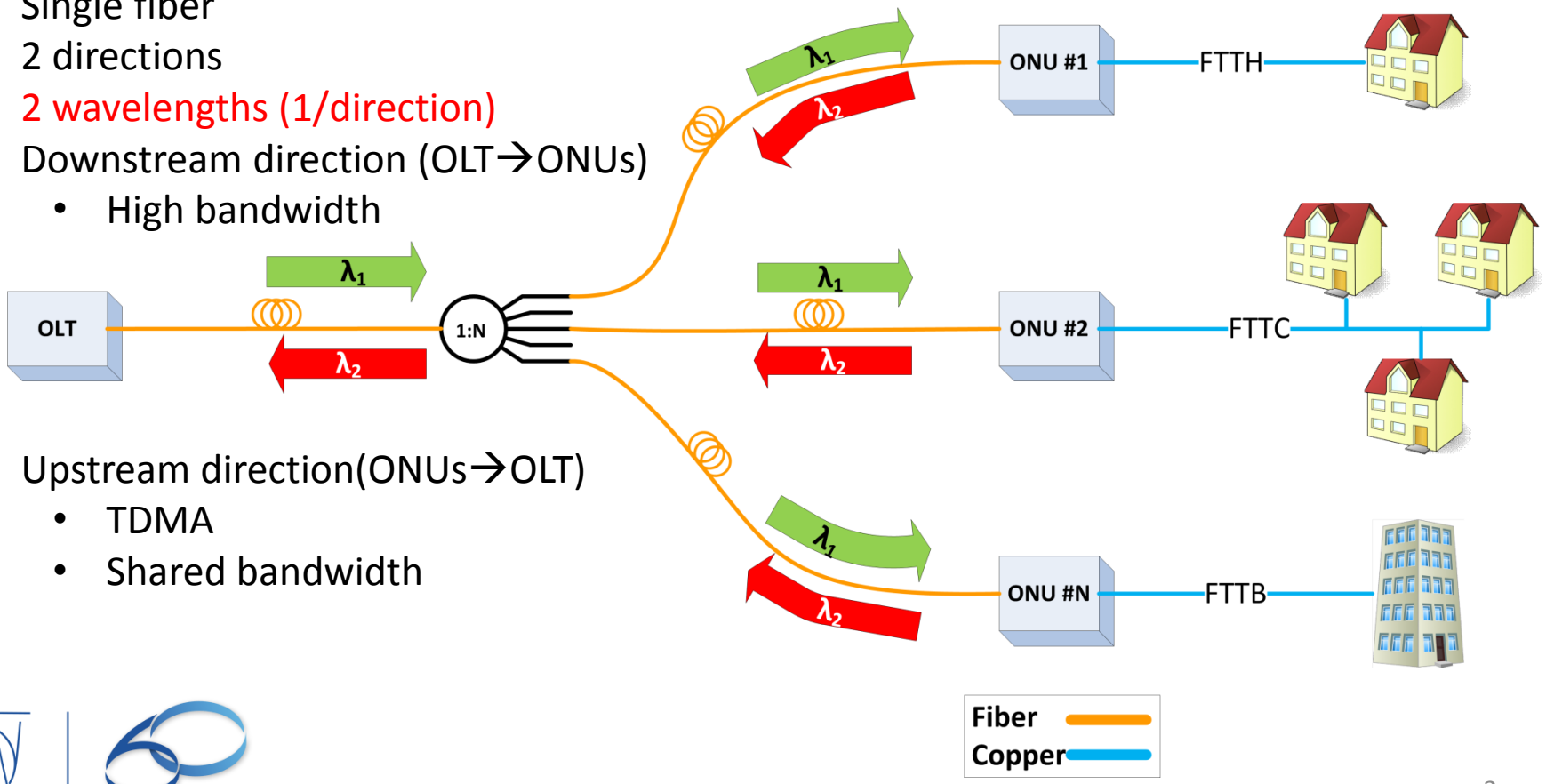
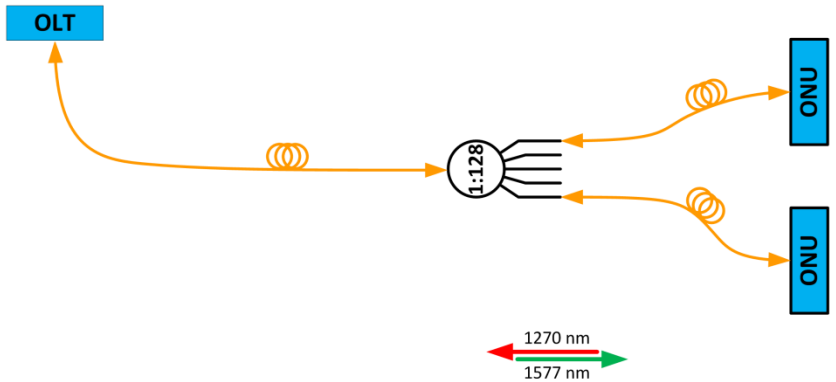
- **PON**: Passive Optical Network
- **FTTH**: Fiber To The Home
- Single fiber
- 2 directions
- 2 wavelengths (1/direction)
- Downstream direction (OLT→ONUs)
  - High bandwidth
- Upstream direction(ONUs→OLT)
  - TDMA
  - Shared bandwidth



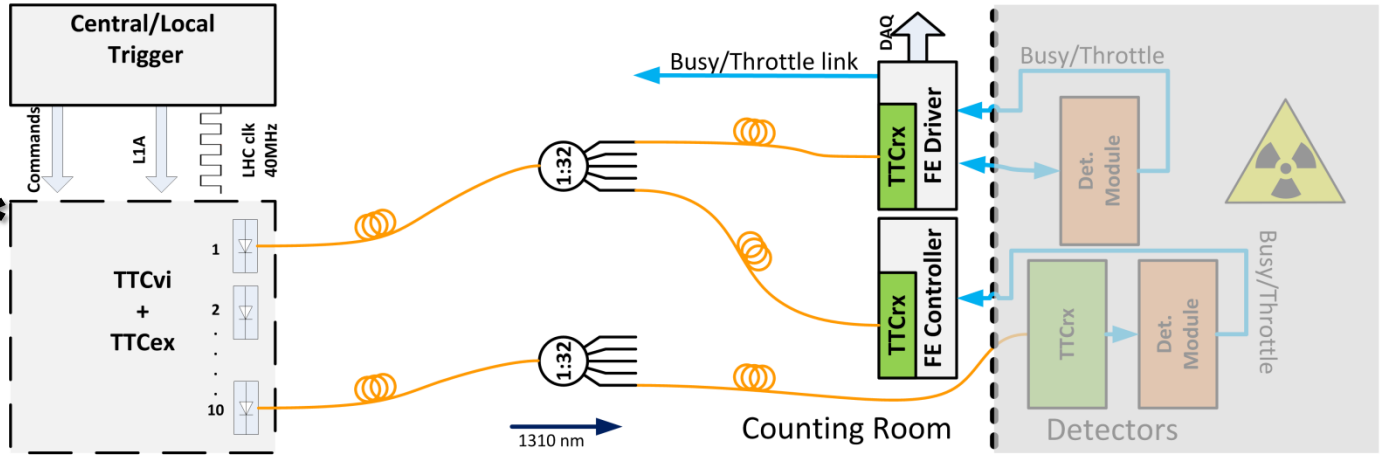
A TTC upgrade proposal using bidirectional 10G-PON FTTH technology

PON



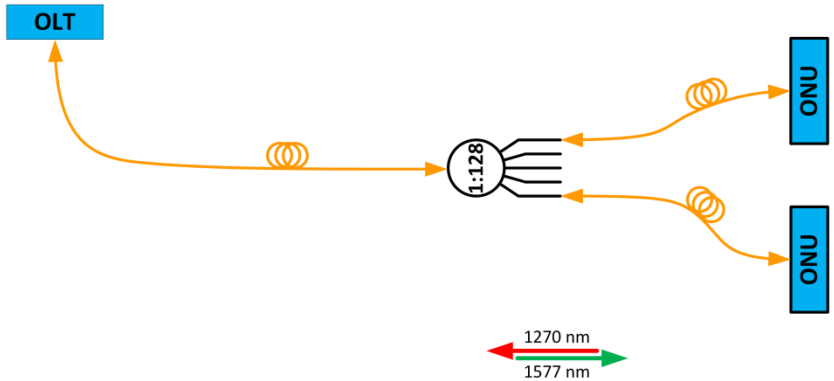
A TTC upgrade proposal using bidirectional 10G-PON FTTH technology

Current TTC*



*TTC: Timing, Trigger & Control

PON



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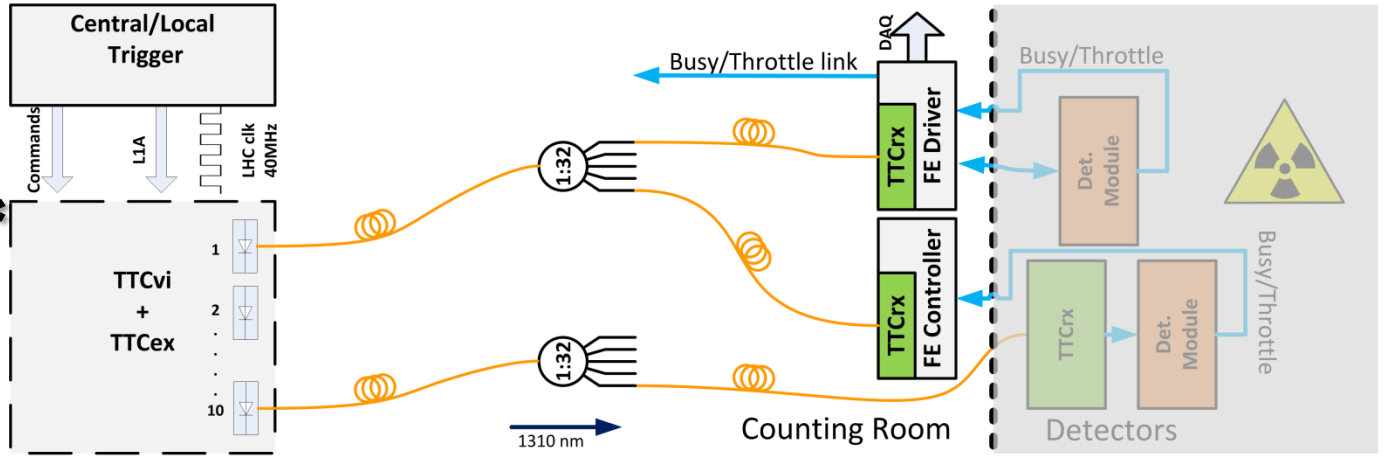

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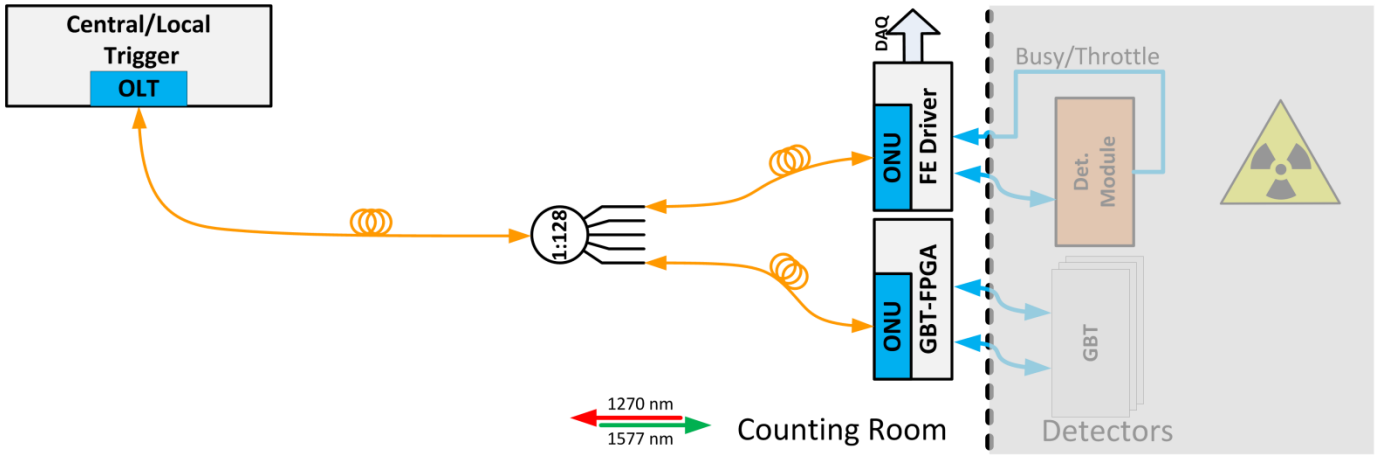
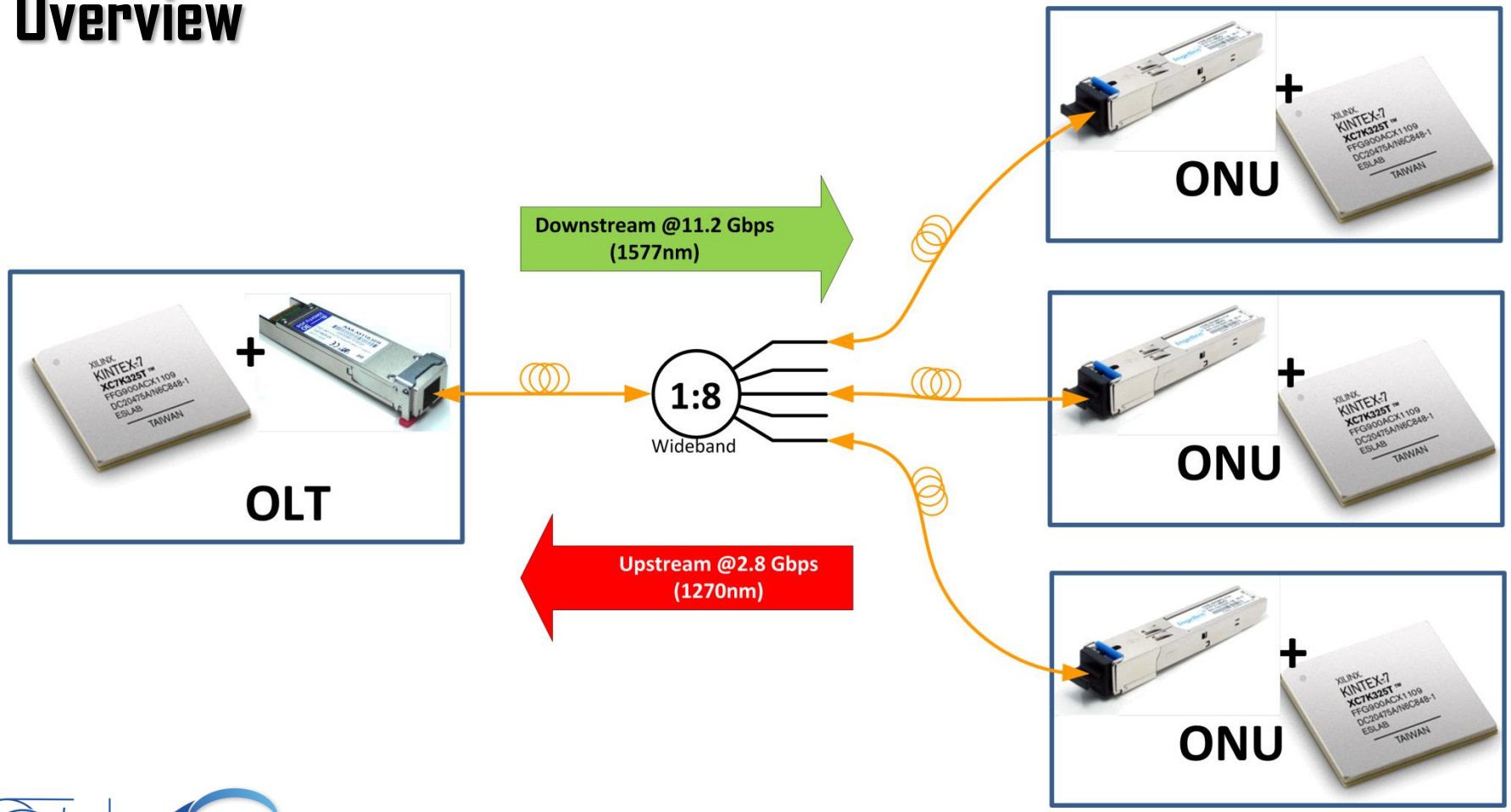


The 10G TTC-PON demonstrator

Overview



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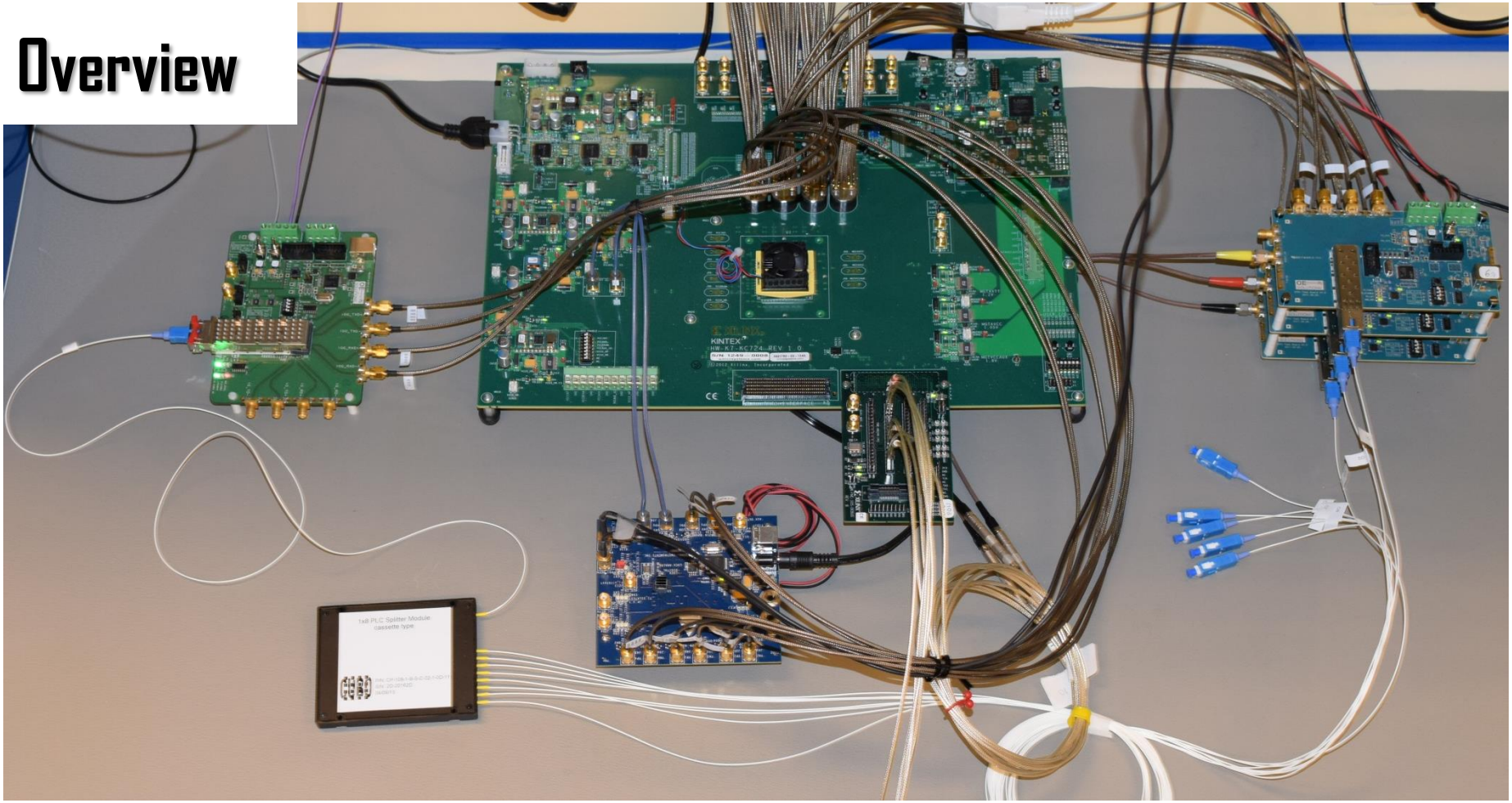

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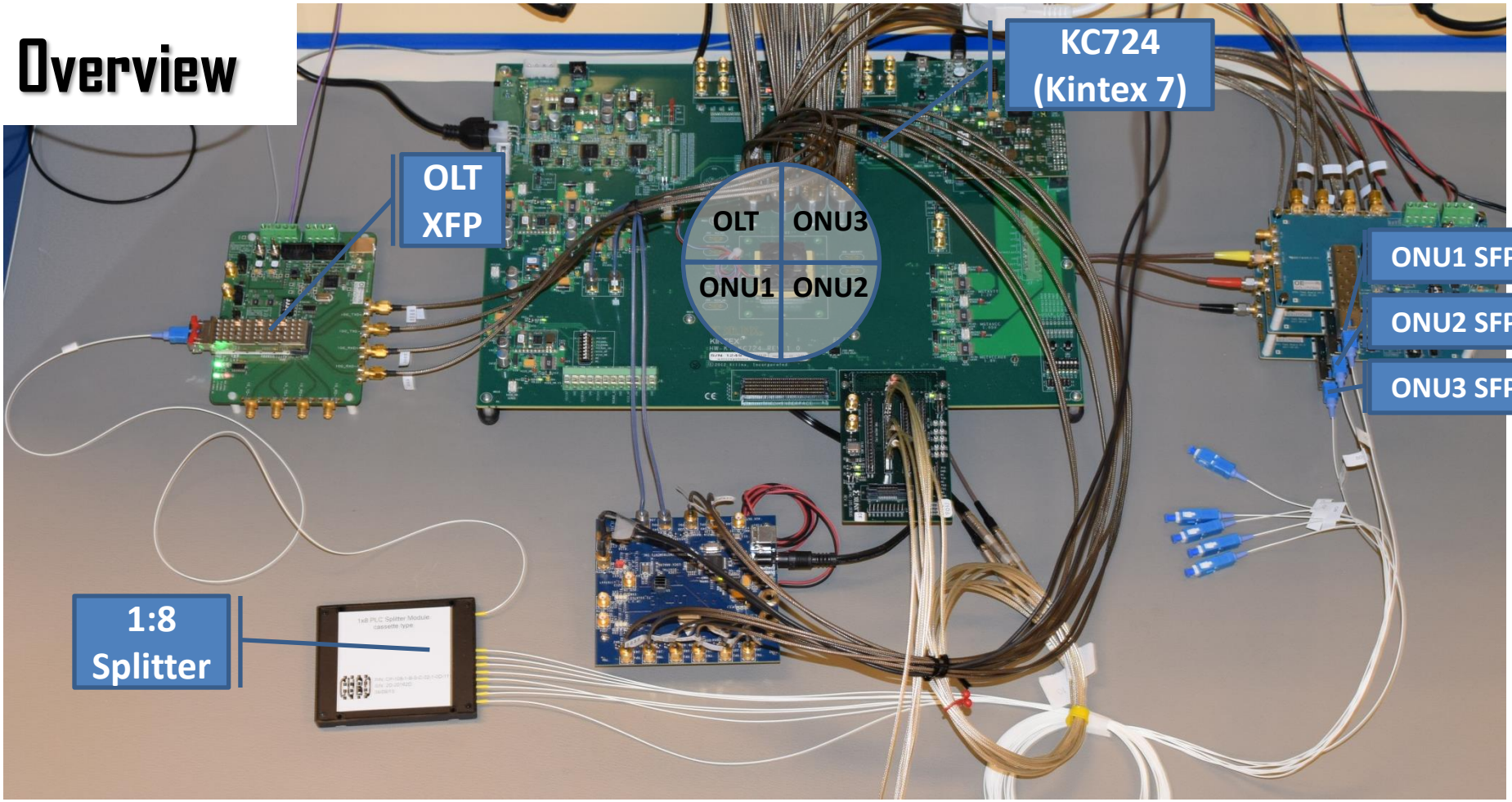
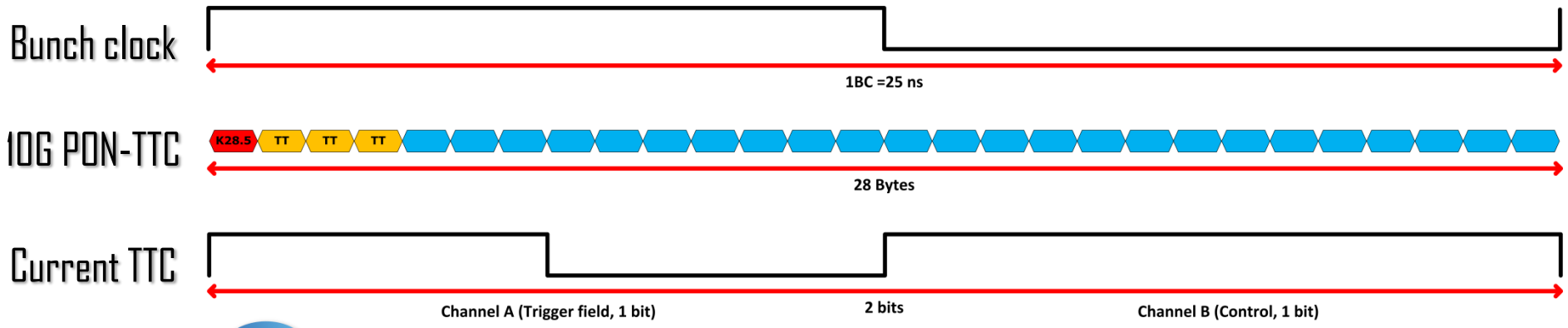


Downstream path

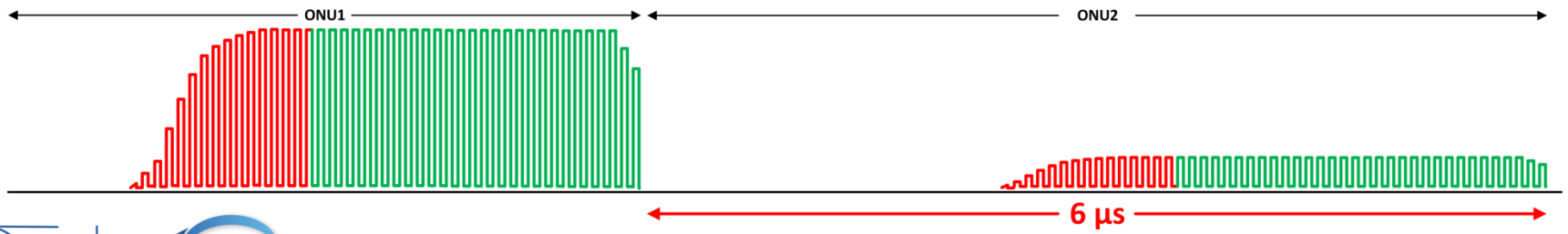
- Broadcast
- LHC Bunch Clock (BC) synchronous
- 11.2Gbps serial link
- 8b/10b encoded, K28.5 comma
- Payload: 216bits (27bytes) per BC
- Latency: 75ns (Comparable to current TTC)



Upstream: Customizing the FTTH standard

Principle

Framing:	FTTx	
Protocol	TDMA	
Hardware	PON Specific ASICs	
Downstream/Upstream clocking	Asynchronous	
Token passed by …	OLT	
Burst recovery/alignment	CDR	
Dynamic Range	>25dB	
Guard Time	500ns	
Training Time	500ns	
Payload Data	3-5µs	
Waiting Time for 128 ONUs (Busy)	~0,8 ms	



Upstream: Customizing the FTTH standard

Principle

Not optimal for busy/throttle use

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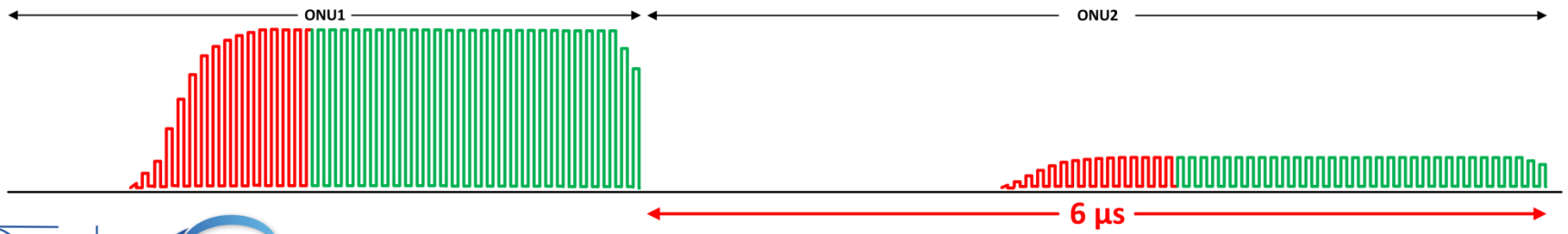

Upstream: Customizing the FTTH standard

Principle

Framing:	FTTx	TTC-PON
Protocol	TDMA	TDMA
Hardware	PON Specific ASICs	FPGAs
Downstream/Upstream clocking	Asynchronous	Synchronous
Token passed by …	OLT	ONUs
Burst recovery/alignment	CDR	Oversampling
Dynamic Range	>25dB	
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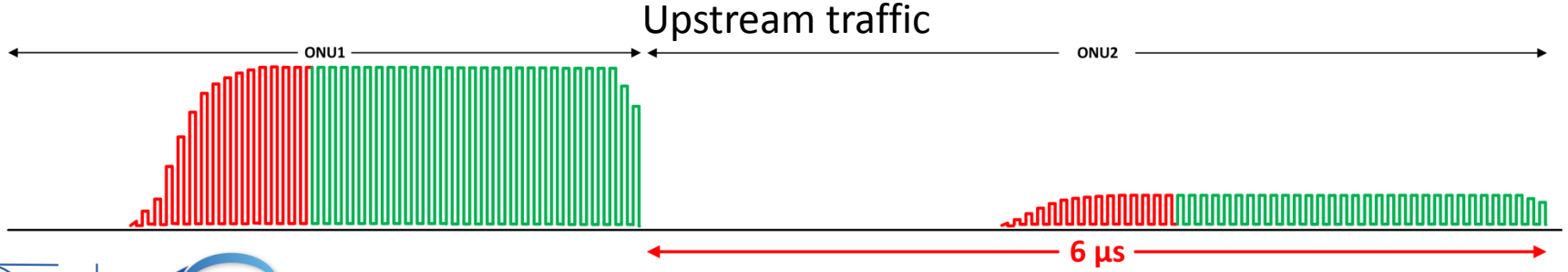

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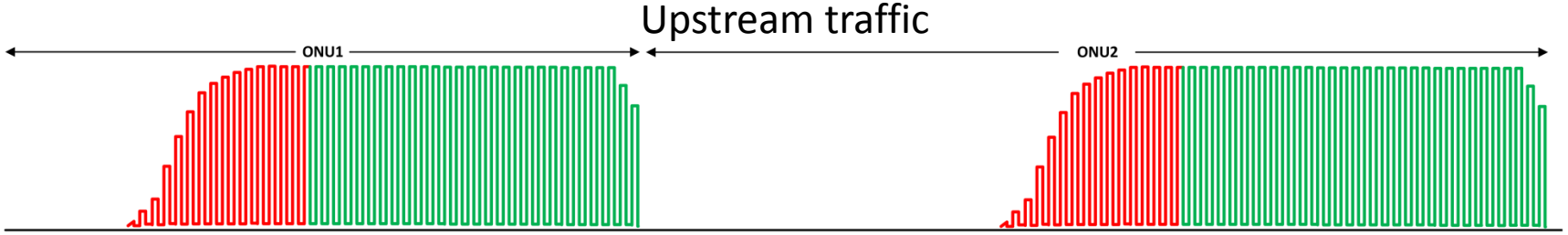

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Dynamic Range	>25dB	Small (<6dB)
Guard Time	500ns	3,57ns
Training Time	500ns	
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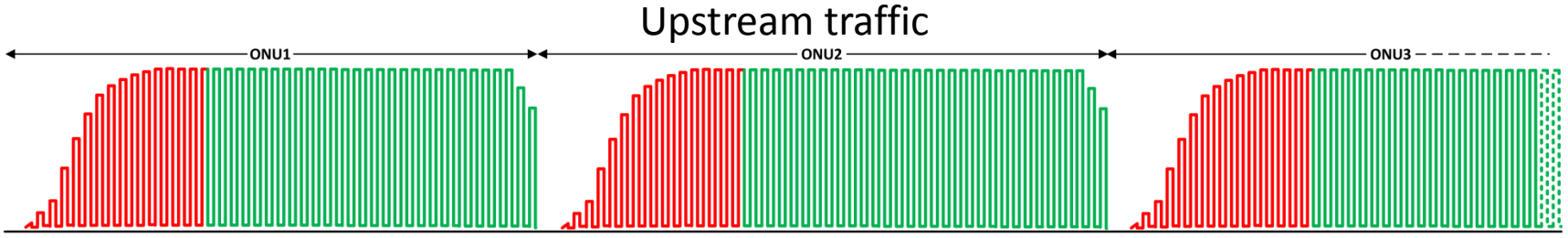
Waiting Time for 128 ONUs (Busy)	~0,8 ms	



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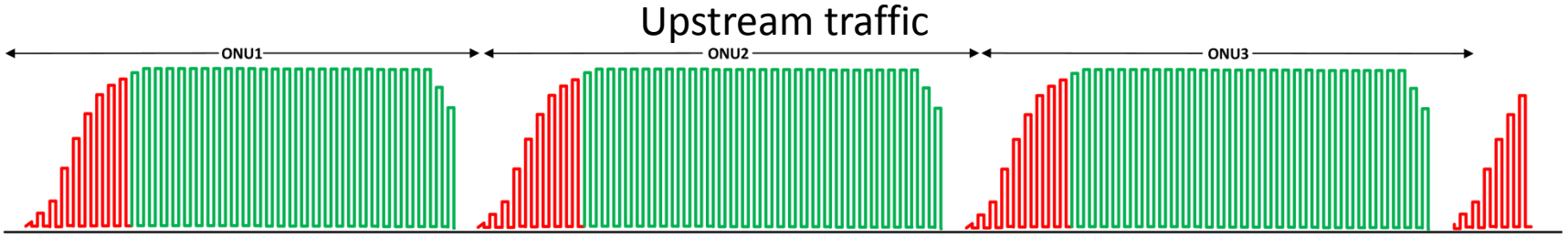
Training Time	500ns	7,14ns
Payload Data	3-5µs	
Waiting Time for 128 ONUs (Busy)	~0,8 ms	



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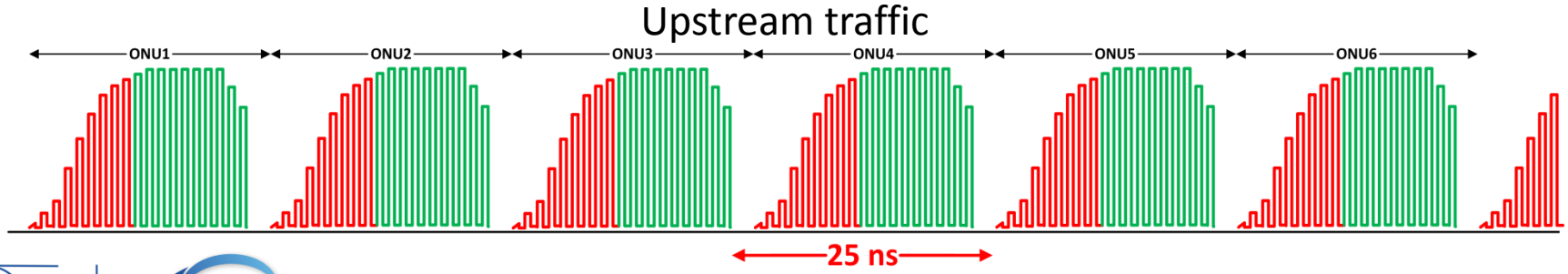
Waiting Time for 128 ONUs (Busy)	~0,8 ms	



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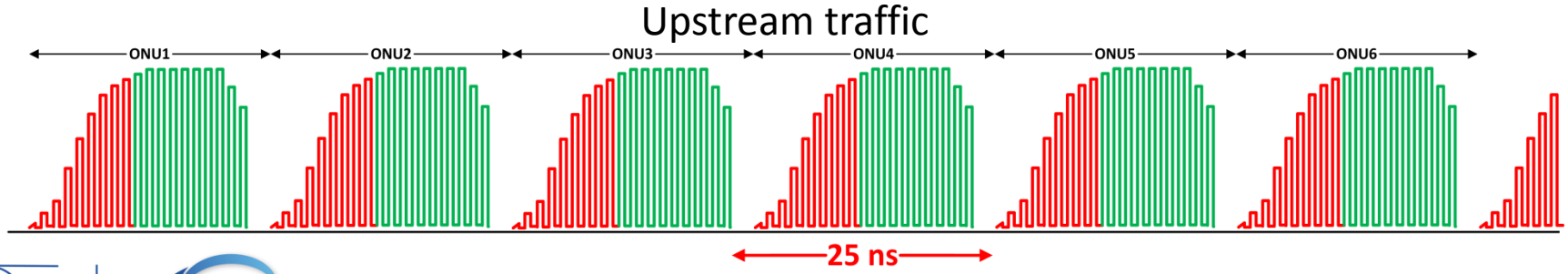
Waiting Time for 128 ONUs (Busy)	~0,8 ms	3,2 µs



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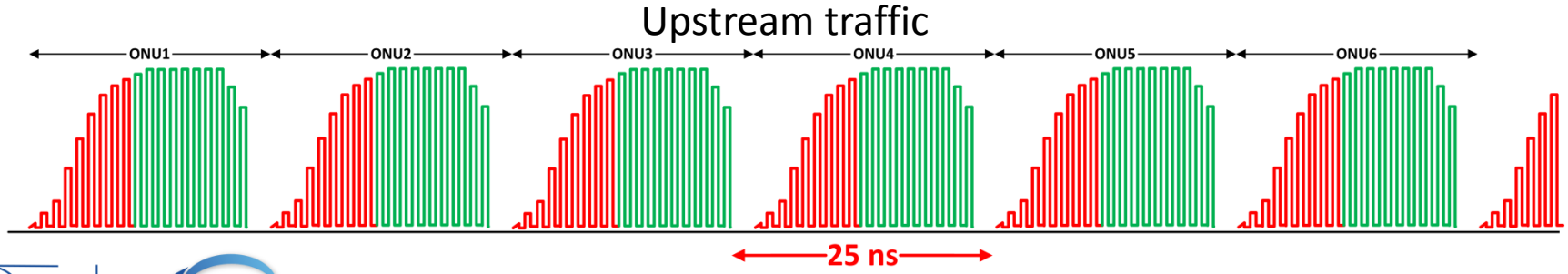
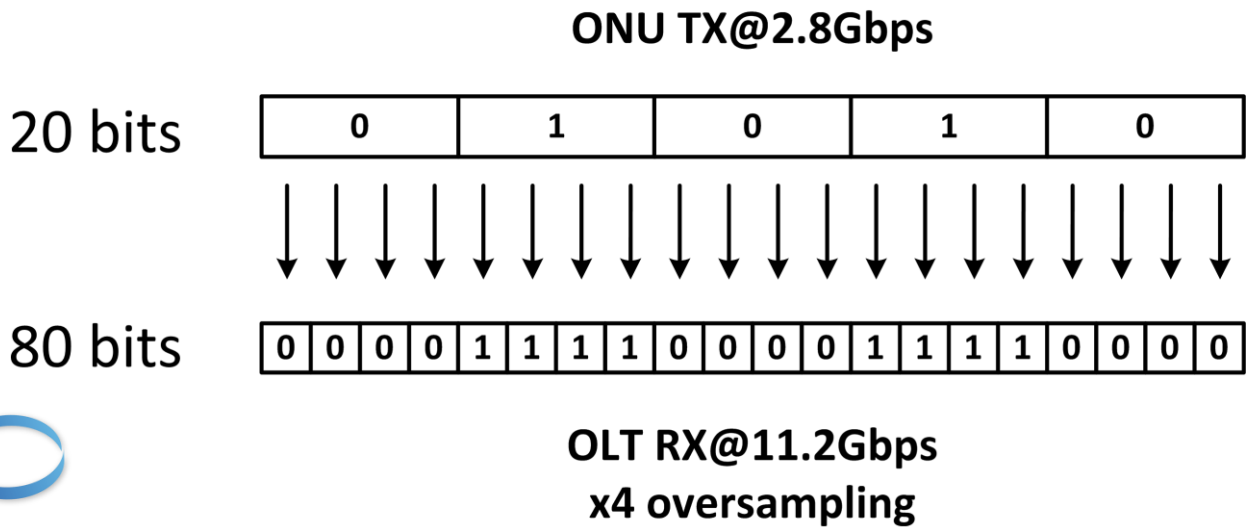


Upstream: Customizing the FTTH standard

- **Link Synchronization**
  - Clock recovery
  - Reuse for Upstream path
- **Calibration**
  - Response time measurement
  - Transmission time adjustment
- **Very fast fine phase alignement**
  - Changing for each ONU
  - No CDR
  - Blind Oversampling scheme

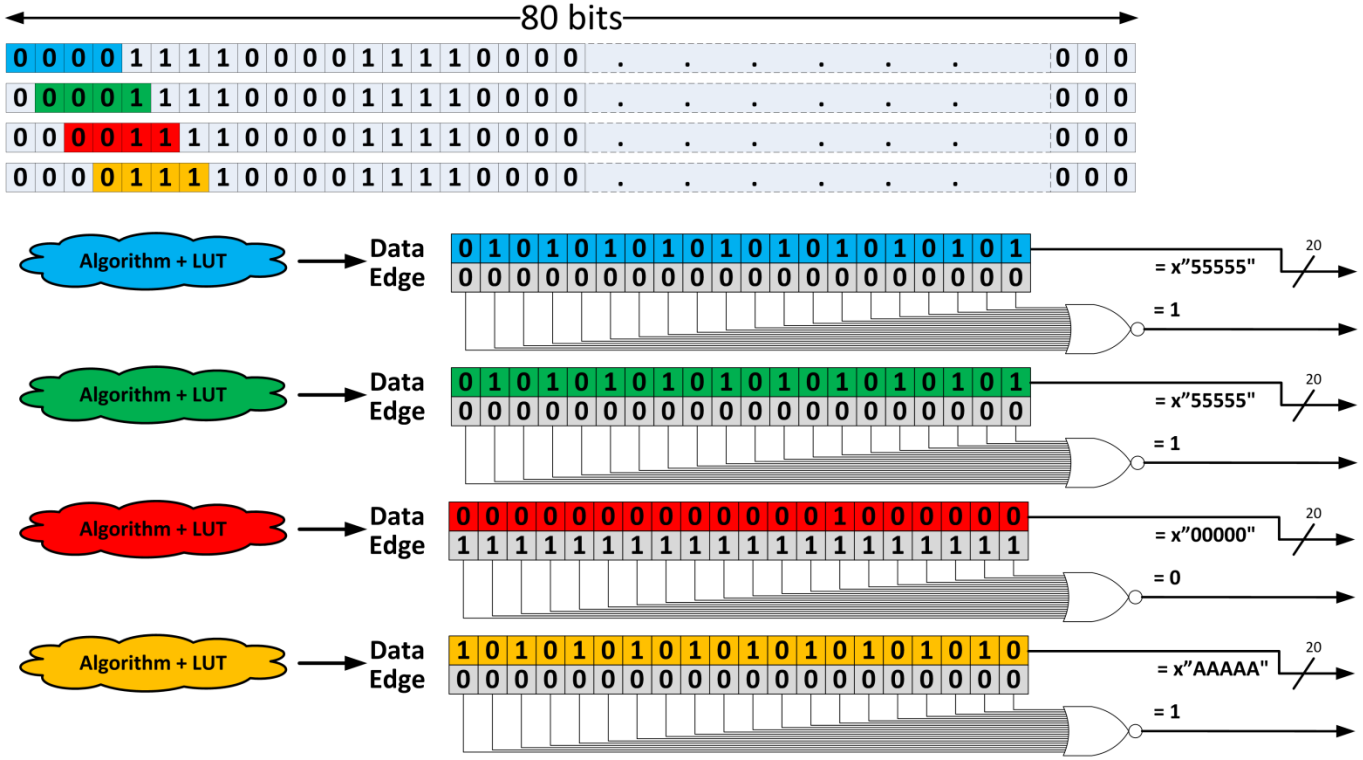
Upstream: Customizing the FTTH standard

- CDR not working with short bursts
- Exploitation of Downstream/Upstream synchronization
- Blindly Oversample x4



Upstream: Customizing the FTTH standard

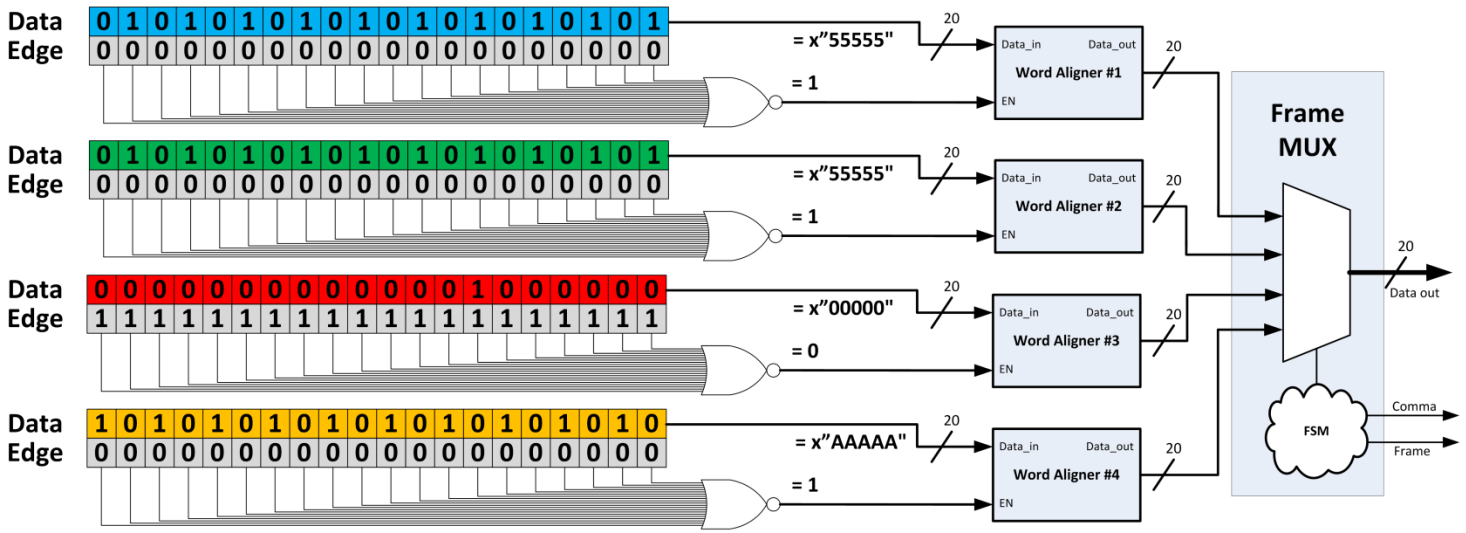
Very fast fine phase alignment



VHDL design: Csaba Soos

Upstream: Customizing the FTTH standard

Very fast fine phase alignment



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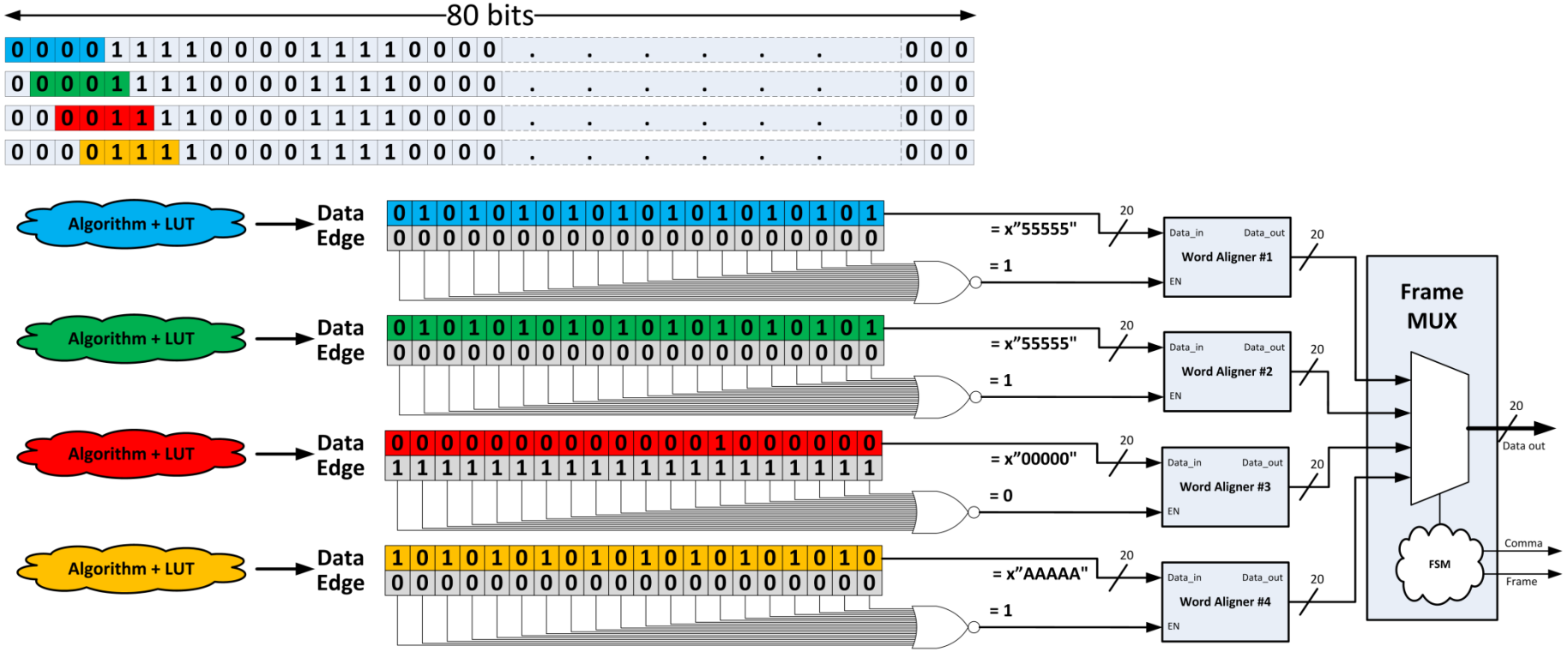
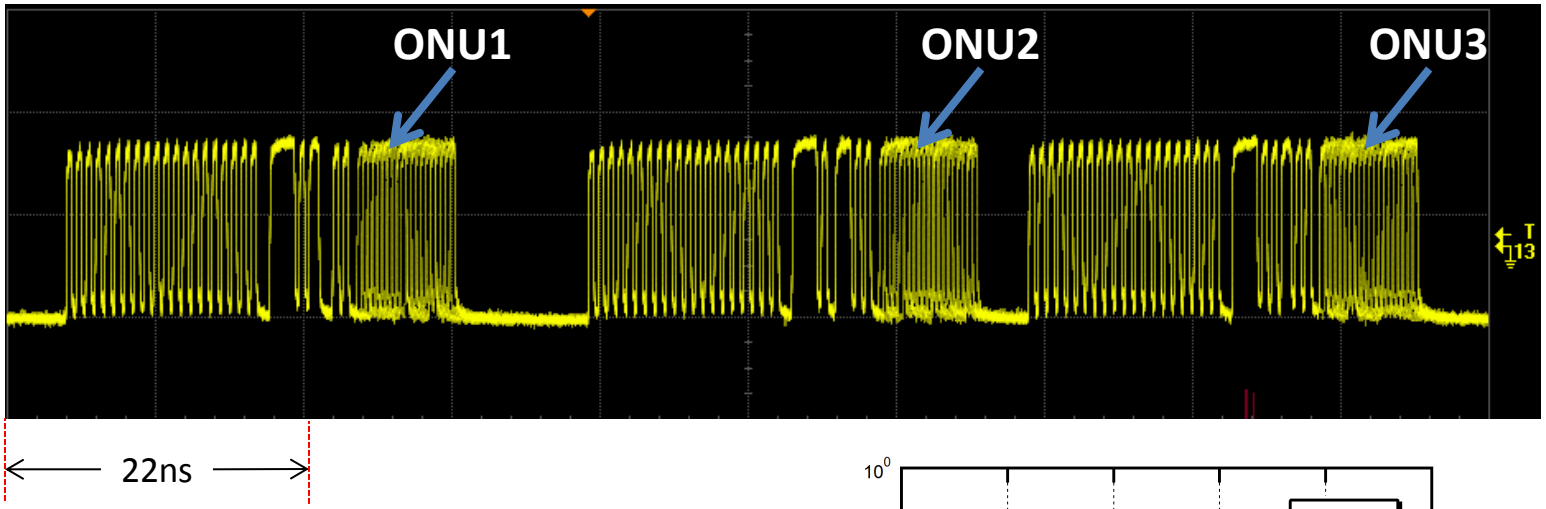


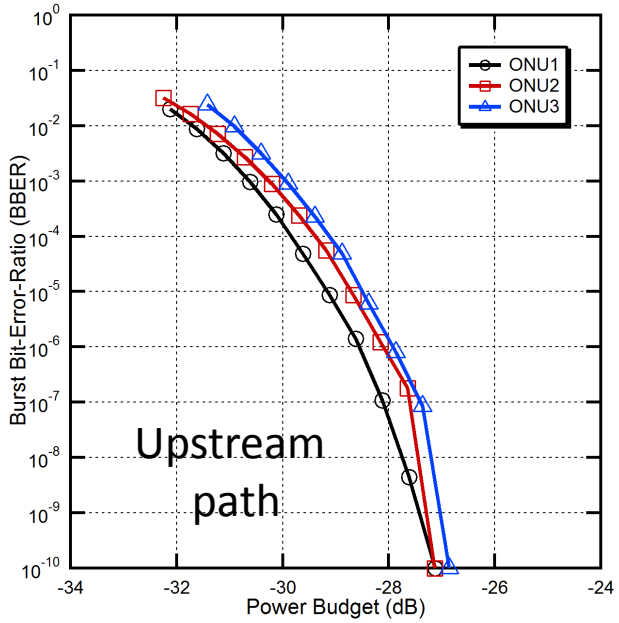
VHDL design: Csaba Soos

Results: Upstream

OLT output

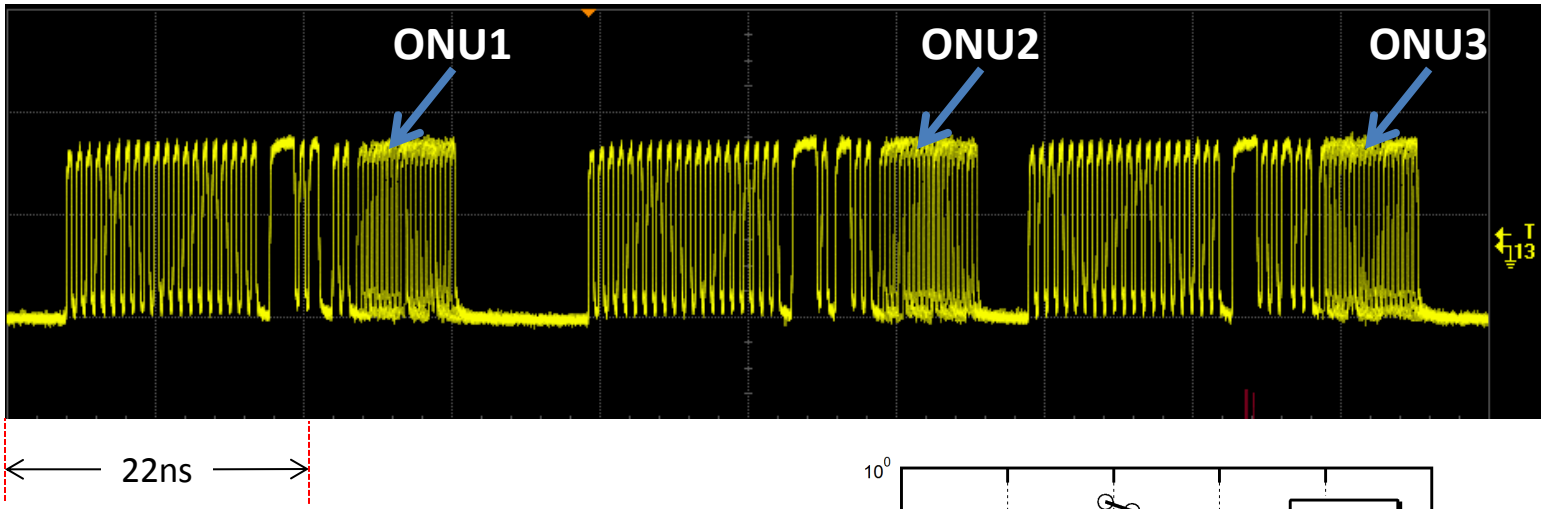


95% stable operation!



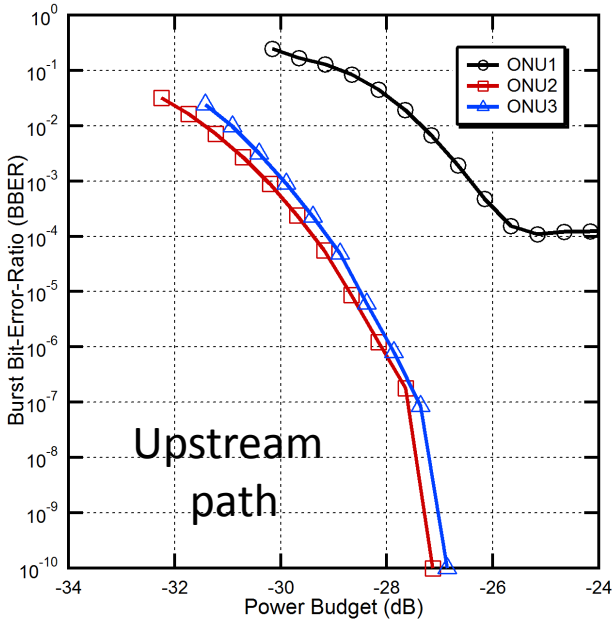
Results: Upstream

OLT output



5% unstable operation…

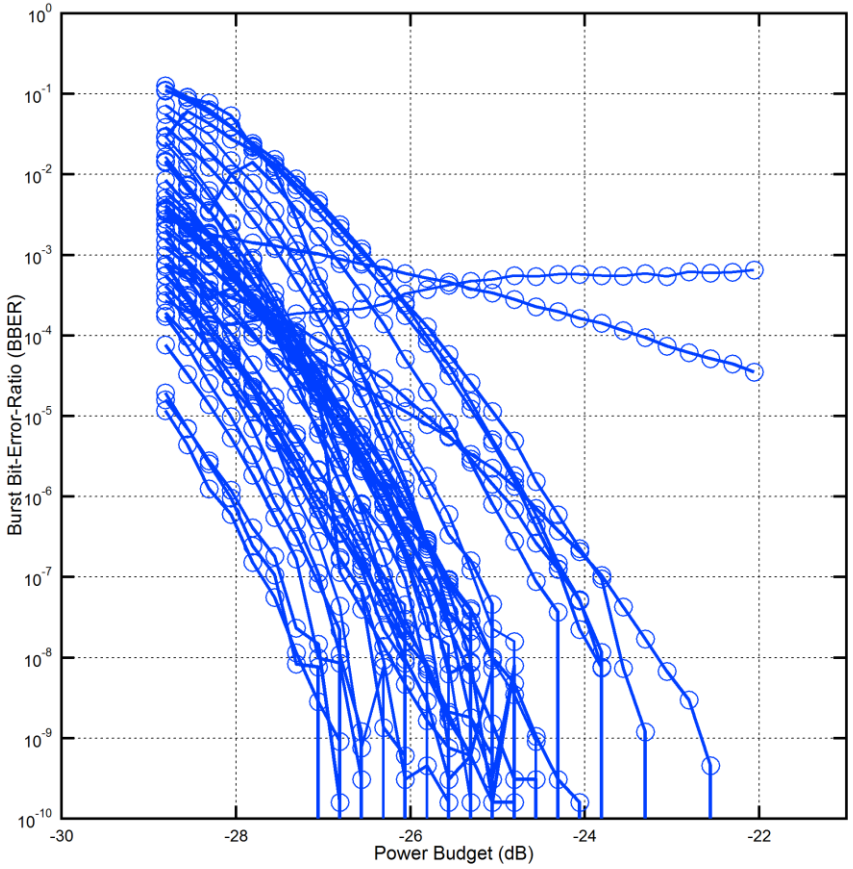
- Phase not always detected and/or
- not correctly chosen



Results: Upstream

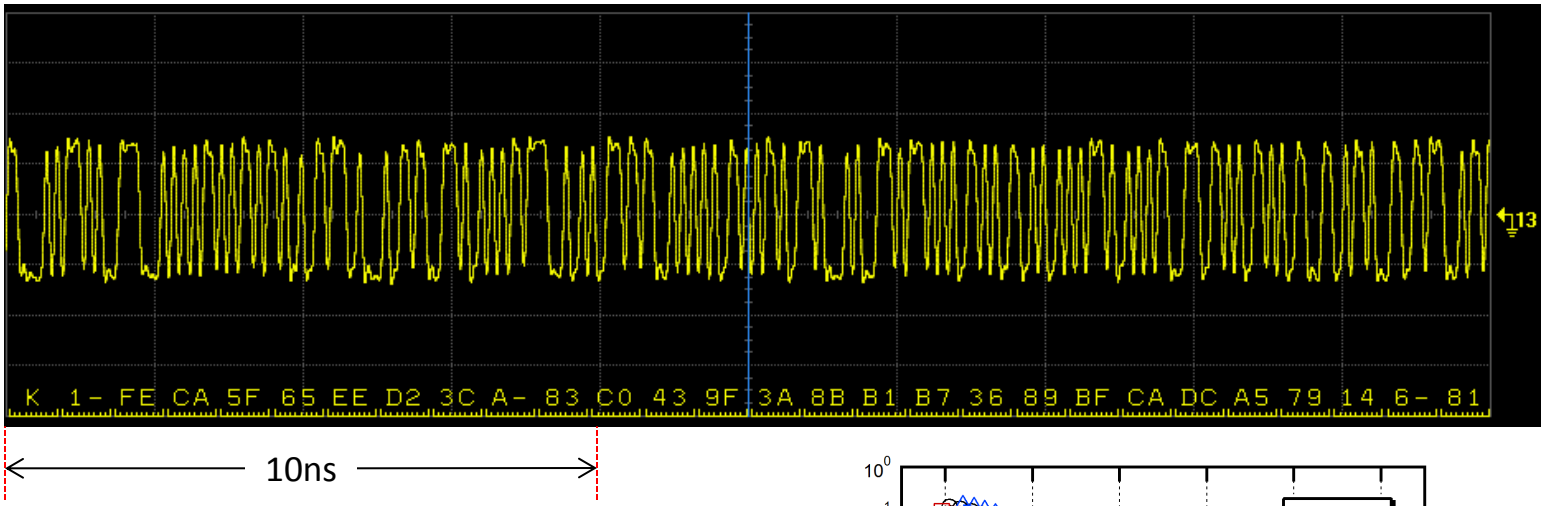
Still 5% of unstable cases.
Possible solutions:

- Different initialisation procedure,
- Precise calibration procedure,
- Logic tweaking
- PHY tweaking
- Higher oversampling rate



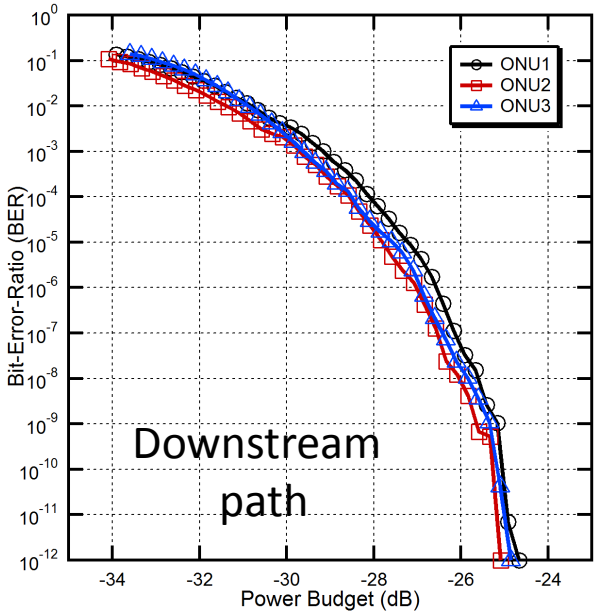
Results: Downstream

ONU output



Typical continuous serial stream @11.2Gbps

Power Budget: ~25dB ➔ 1:128 splitting ratio



Conclusions

- Proposed upgrade of two systems: TTC & "Busy“
- Major improvements over the current system:
  - Low & deterministic latency
  - High quality recovered clock
  - High capacity
- Upstream path introduced
- Scalability + dynamic Software partitioning ability
- Backwards compatible (TTC only, not busy/throttle link)

What's next?

- Reach 100% of good BER plots
- Reduce further the gap and training pattern
- Properly characterize
- Go on the field!
  - Feasibility study for LHCb LS2 (poster session, Federico Alessio's poster)

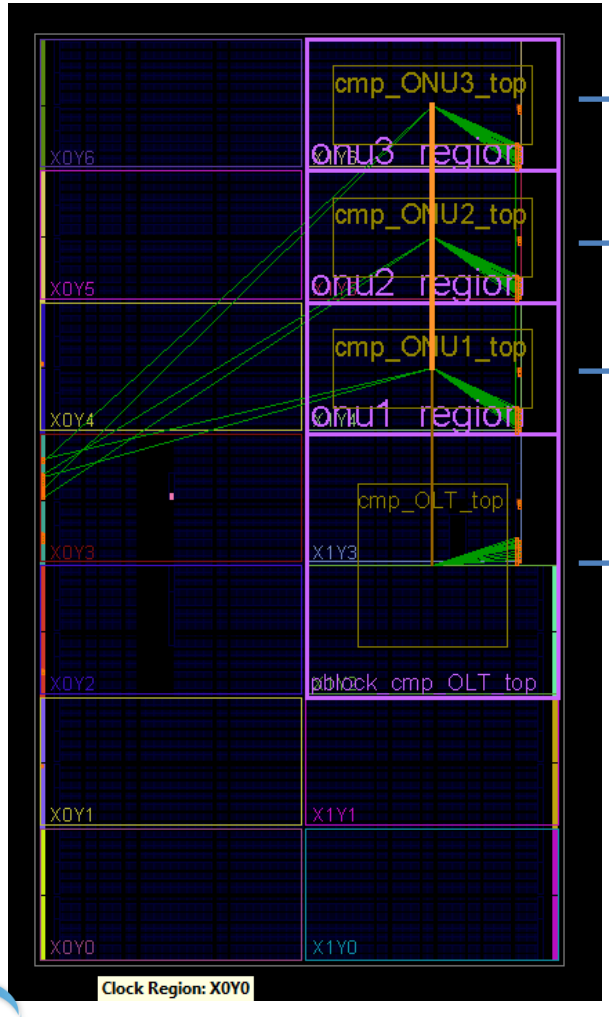
References

- Clock and Timing Distribution in the LHCb Upgraded Detector and Readout System, Federico Alessio, Poster Session, TWEPP 2014
- TTC-PON, migrating from 1G to 10G, BE-Students/Fellows Seminar, 2014
- TTC Upgrade plans, The TTC-PON project , ACES 2014
- *Metrics and Methods for TTC-PON System Characterization* , D. Kolotouros, TWEPP 2013, Perugia
- *TTC-PON, an upgrade proposal for off-detector TTC* , DAQ@LHC 2013
- Distribution of Timing, Trigger and Control signals based on Passive Optical Networks BE-Students/Fellows Seminar
- *A Fully Bidirectional Optical Network with Latency Monitoring Capability for the Distribution of Timing-Trigger and Control Signals in High-Energy Physics Experiments*, I. Papakonstantinou et al., IEEE Transactions on Nuclear Science , 58 (4 PART 1) 1628 - 1640. 10.1109/**TNS**.**2011.2154364**.
- Introduction to the TTC-PON concept @ACES 2011
- *Passive Optical Networks in Particle Physics Experiments*, I. Papakonstantinou, 24th November 2009, PH-ESE Seminar

THANK YOU

BACKUP SLIDES

Separated clock domains



ONU3

ONU2

ONU1

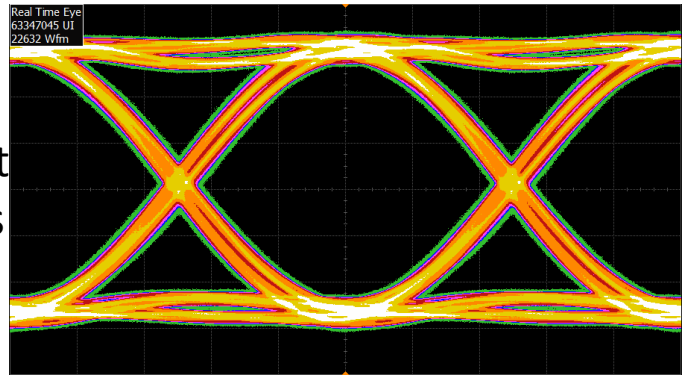
OLT

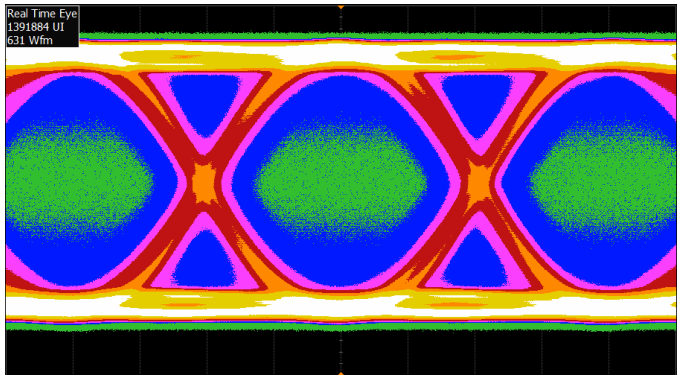
```
########## AREA CONTRAINTS ############
INST "cmp_ONU3_top" AREA_GROUP = "onu3_region";
AREA_GROUP "onu3_region" RANGE=CLOCKREGION_X1Y6:CLOCKREGION_X1Y6;
INST "cmp_ONU2_top" AREA_GROUP = "onu2_region";
AREA_GROUP "onu2_region" RANGE=CLOCKREGION_X1Y5:CLOCKREGION_X1Y5;
INST "cmp_ONU1_top" AREA_GROUP = "onu1_region";
AREA_GROUP "onu1_region" RANGE=CLOCKREGION_X1Y4:CLOCKREGION_X1Y4;

INST "cmp_OLT_top" AREA_GROUP = "pblock_cmp_OLT_top";
AREA_GROUP "pblock_cmp_OLT_top" RANGE=CLOCKREGION_X1Y2:CLOCKREGION_X1Y3;
```

Datarate selection

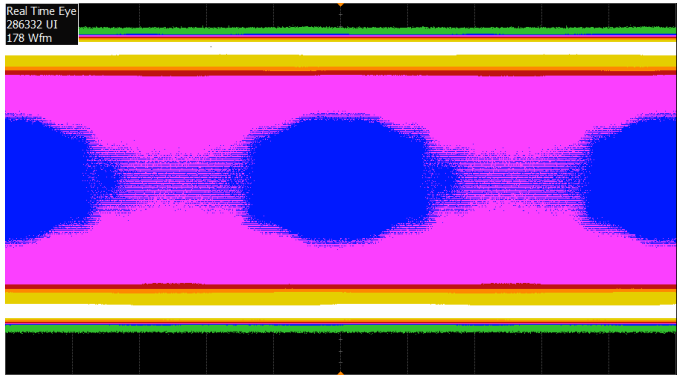
ONU output @11.2Gbps





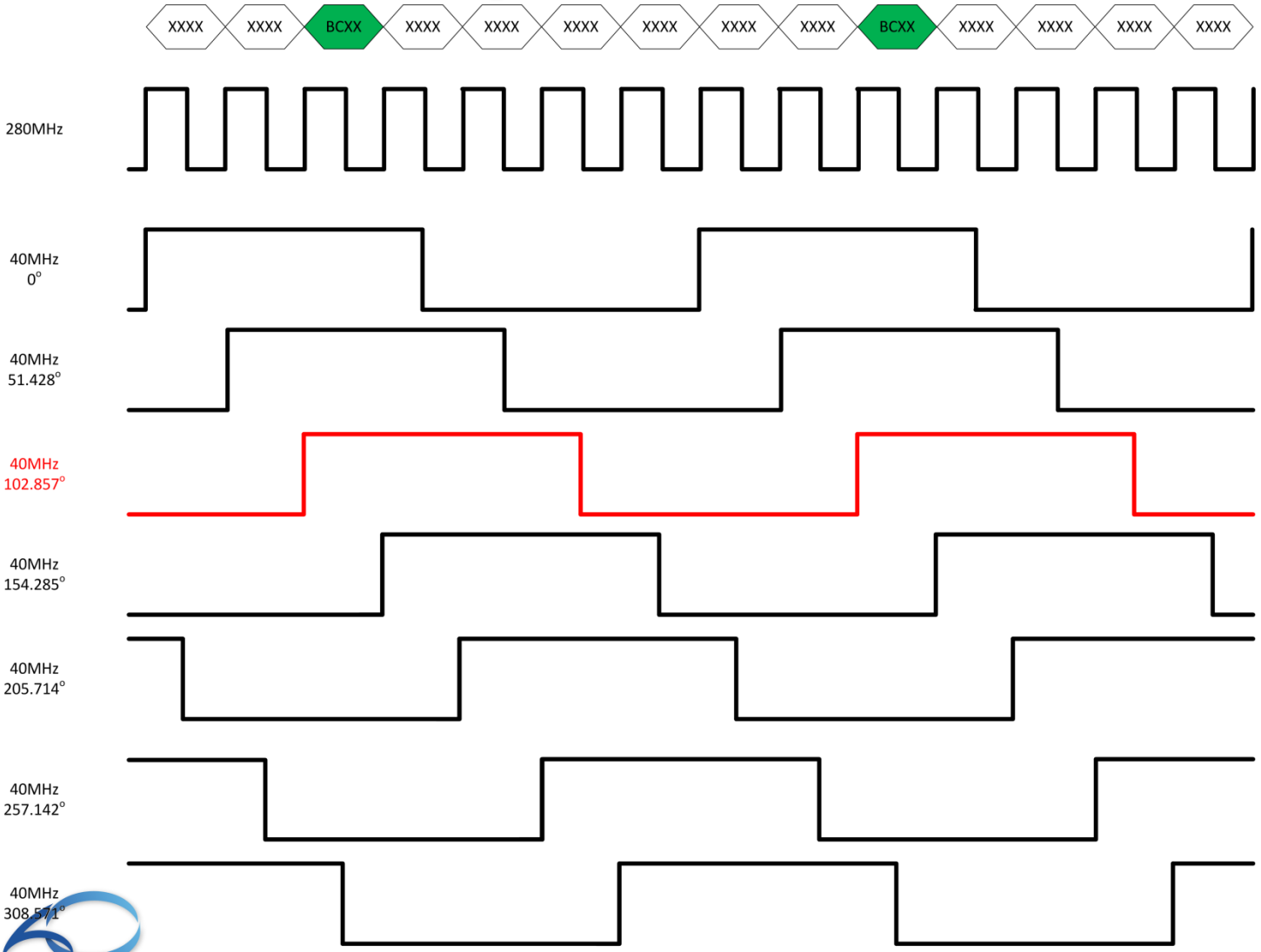
ONU output @8Gbps

ONU output @9.6Gbps



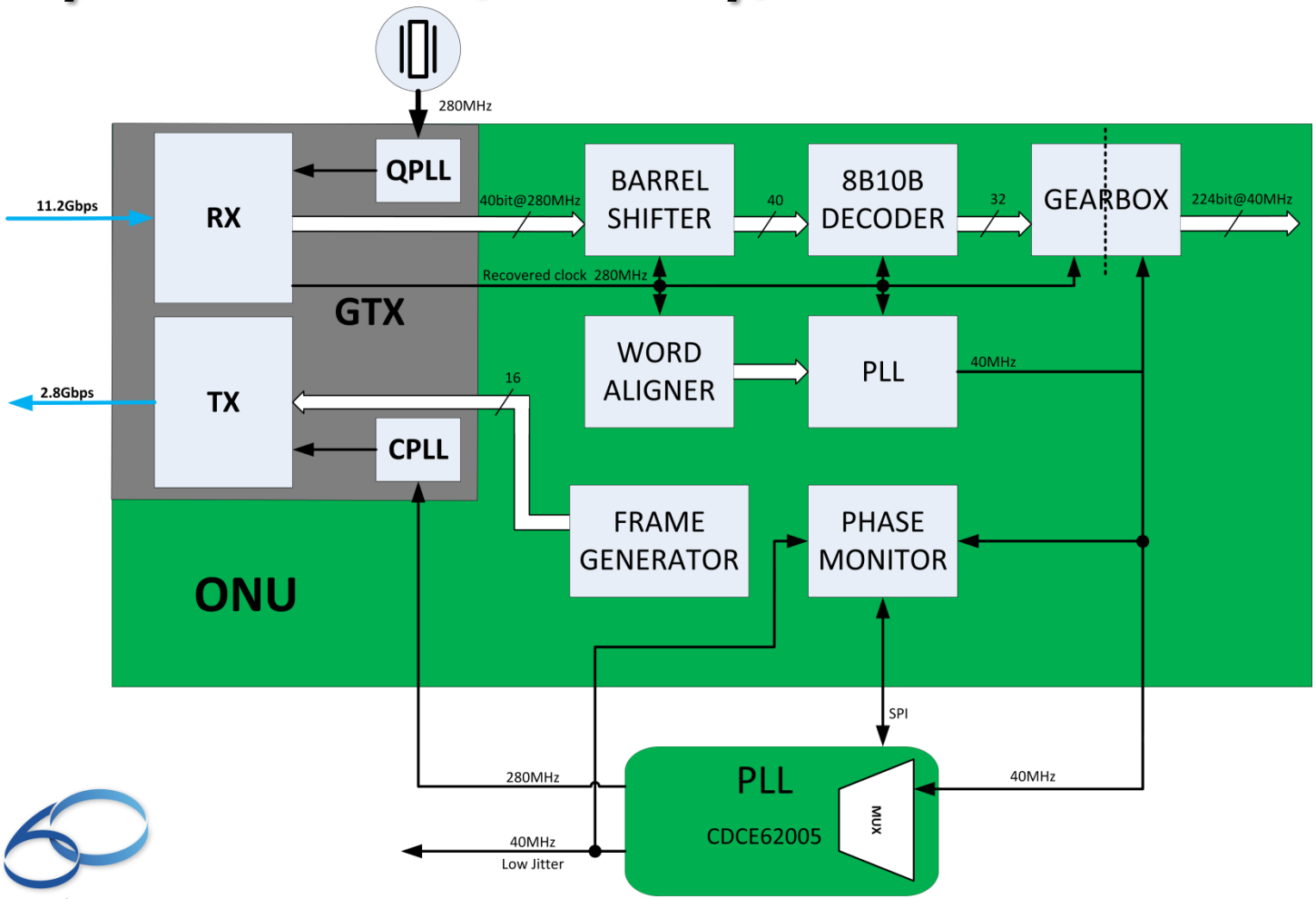
ONU output @6.4Gbps

Possible phases of 40MHz



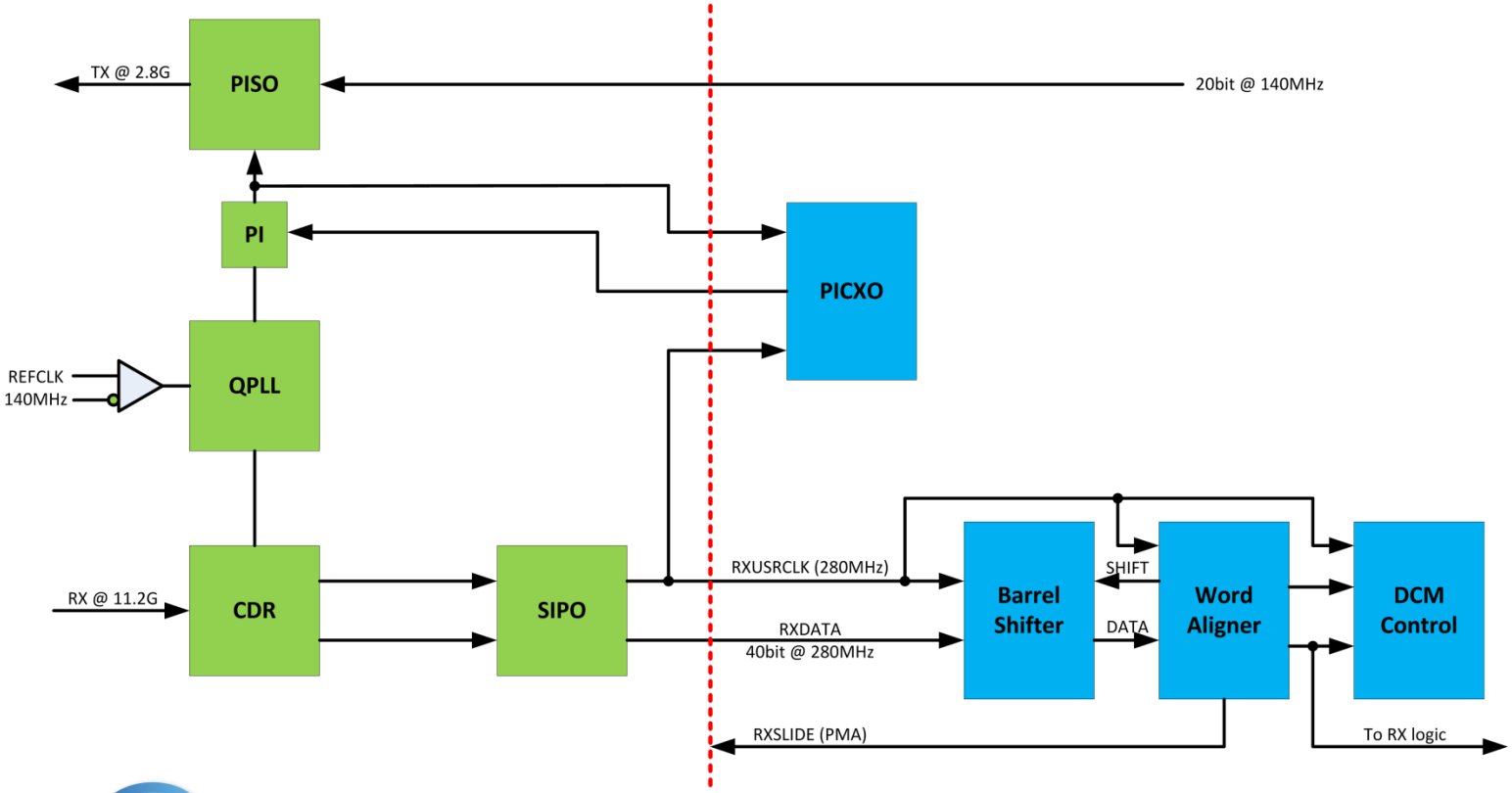
Upstream: Customizing the FTTH standard

Link synchronization (Externally)



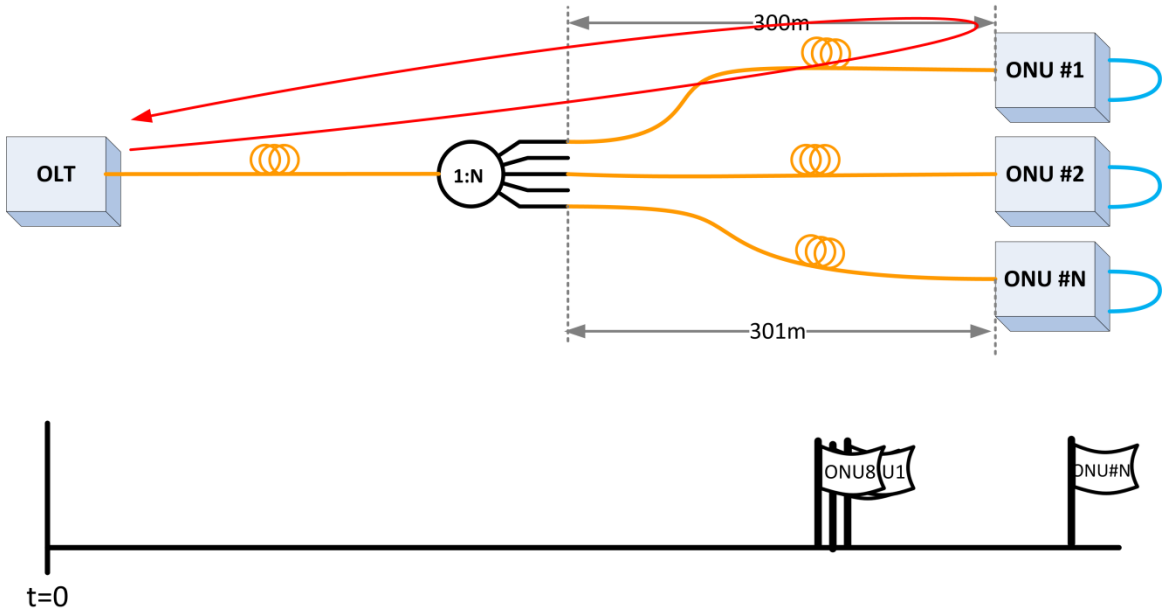
Upstream: Customizing the FTTH standard

Link synchronization (Internally)

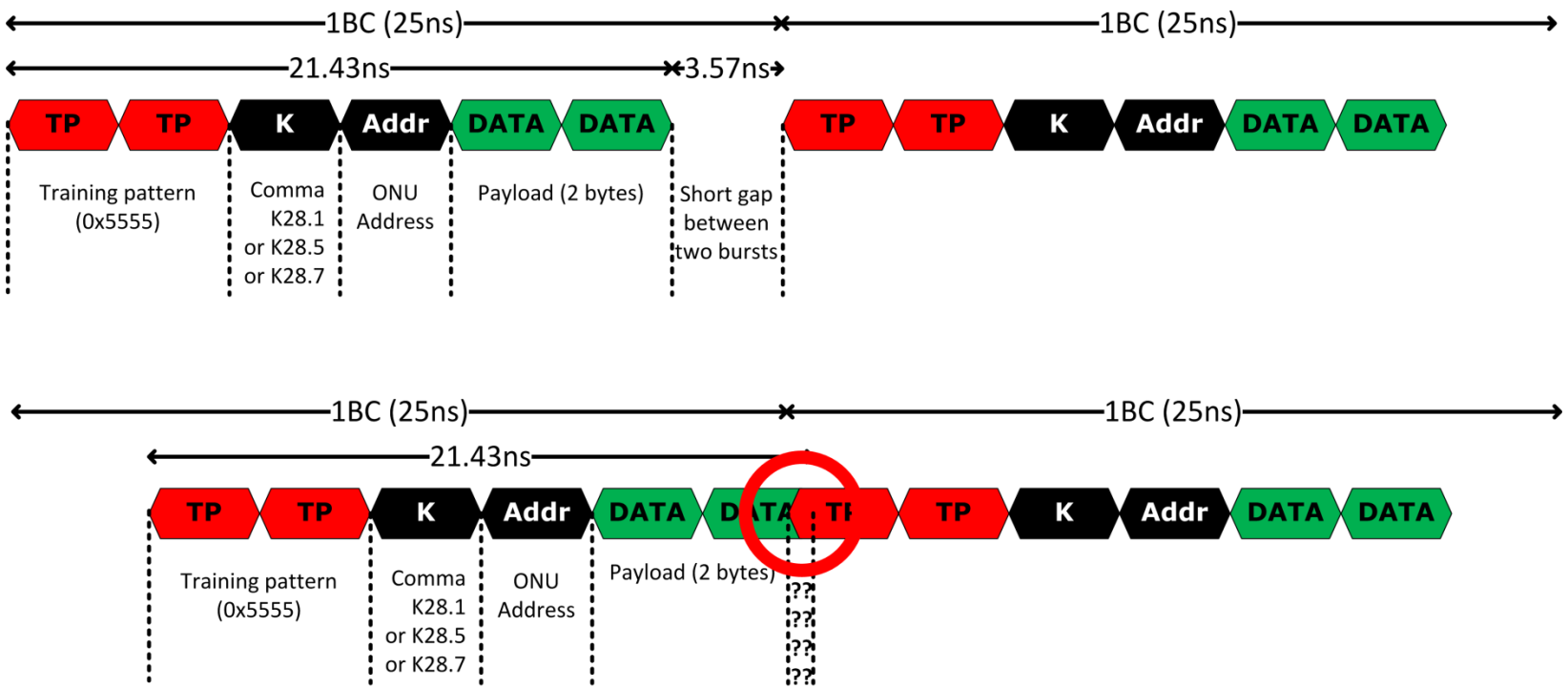


VHDL design: Csaba Soos

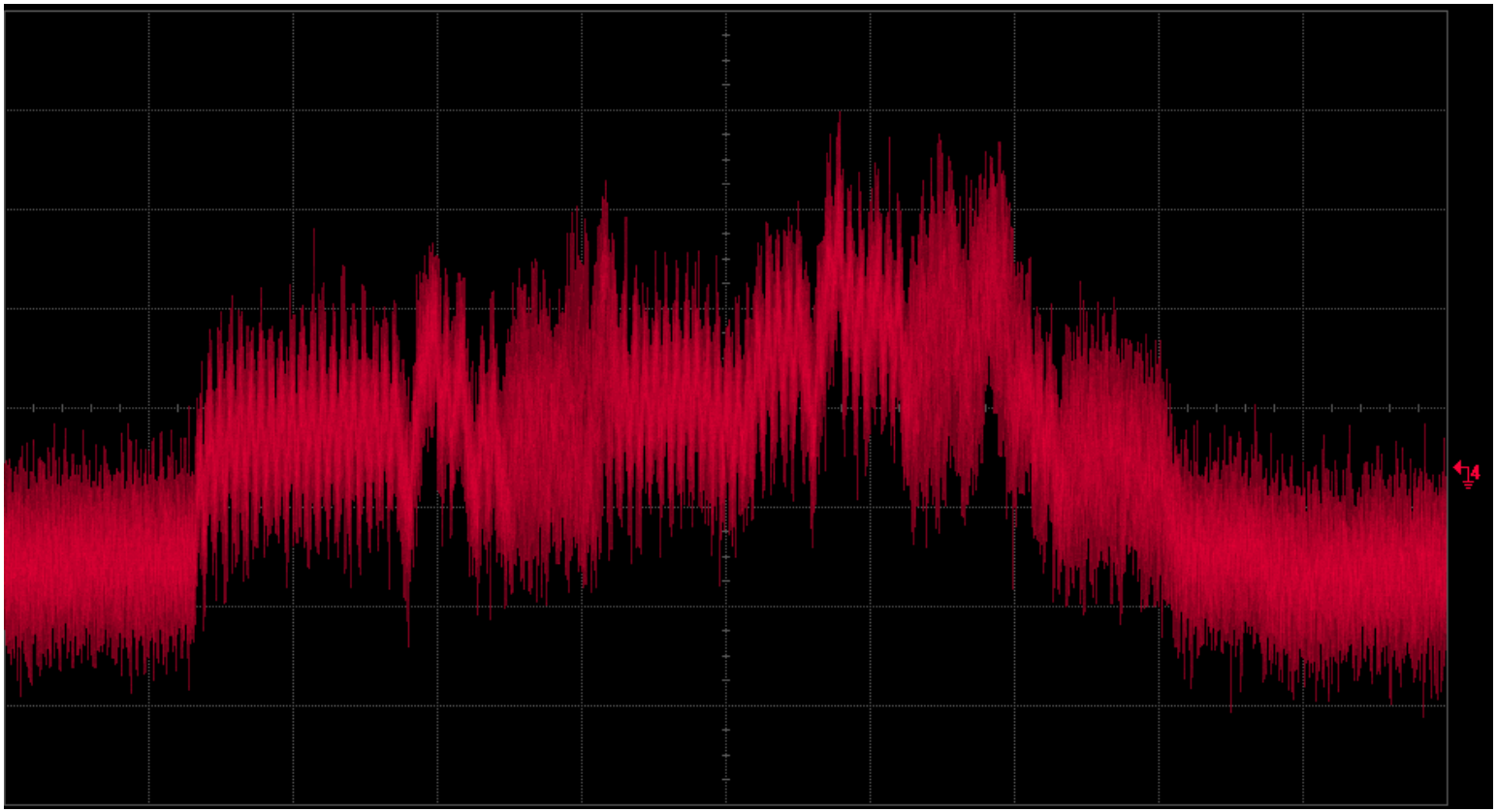
Why calibration is needed (1/3)



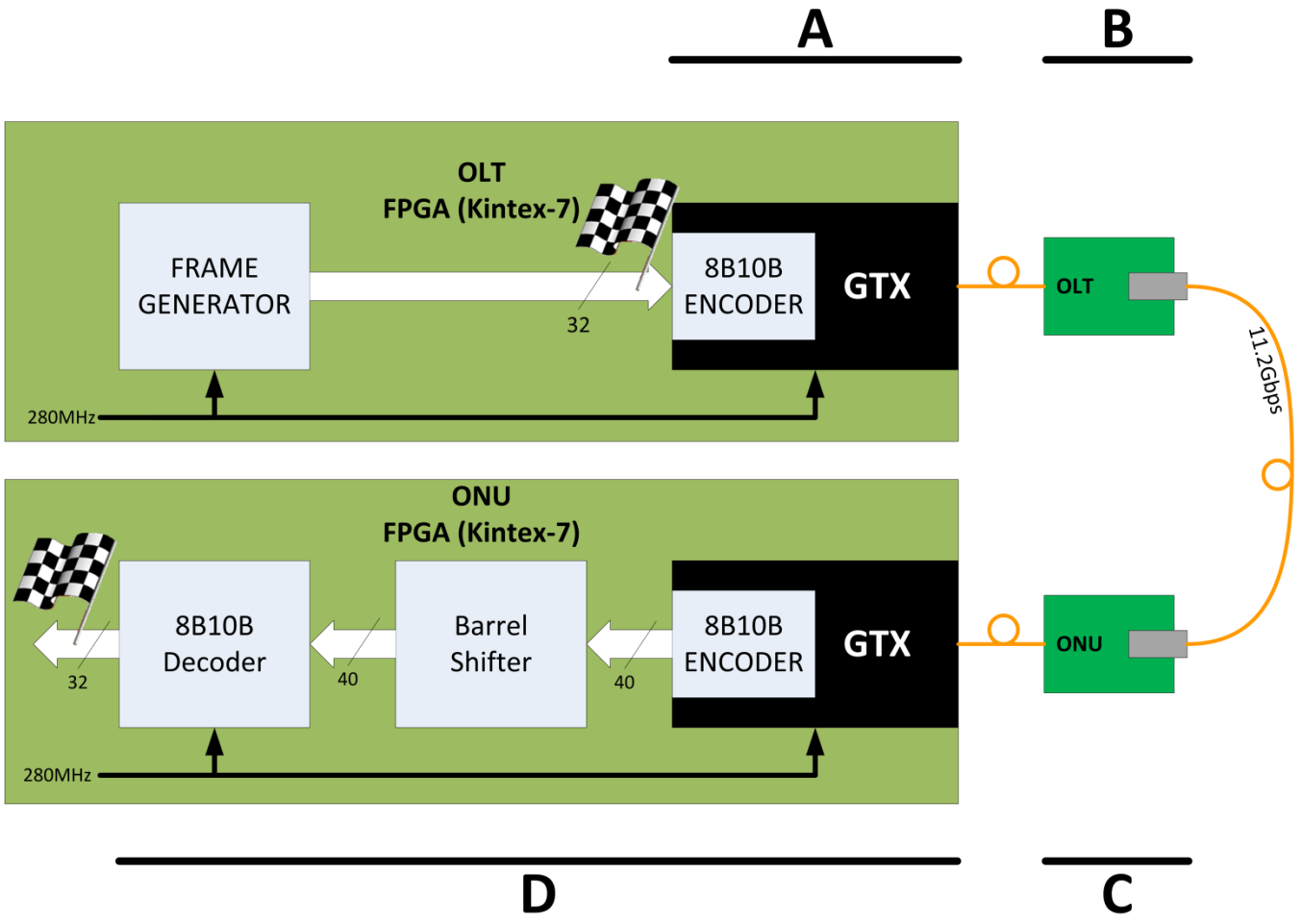
Why calibration is needed (2/3)



Why calibration is needed (3/3)

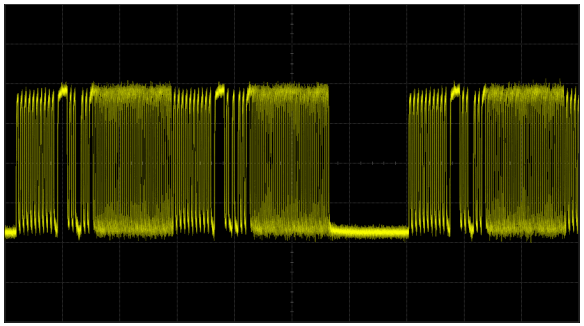


Downstream Latency

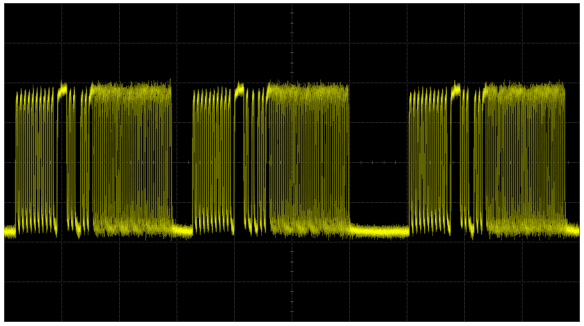


Downstream latency =A + B + C + D = 73ns

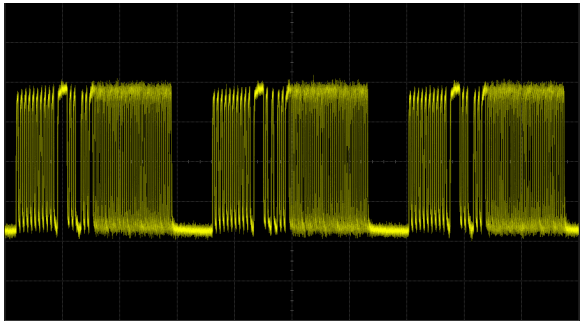
Blind Oversampler testing



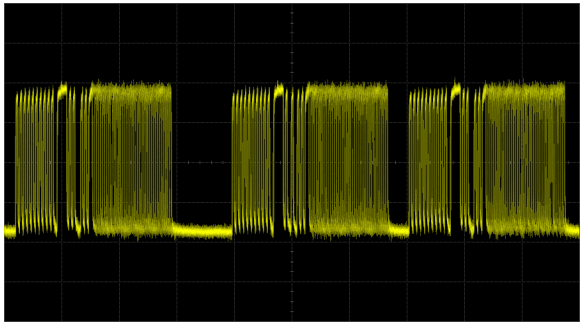
0 bits



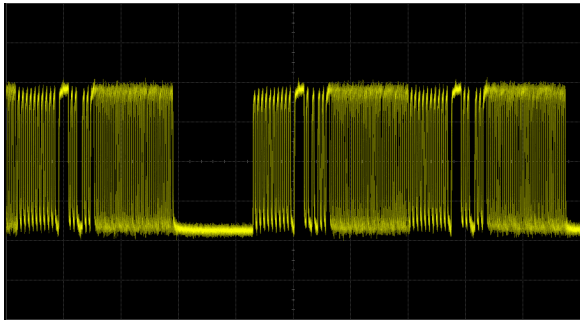
10 bits



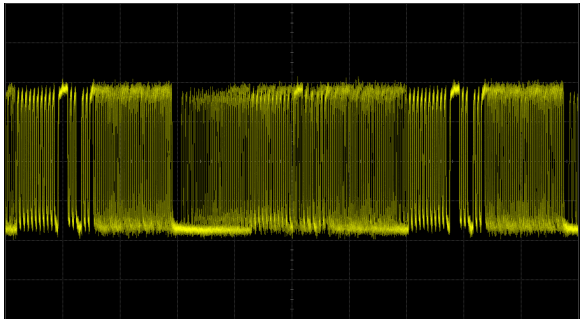
20 bits



30 bits

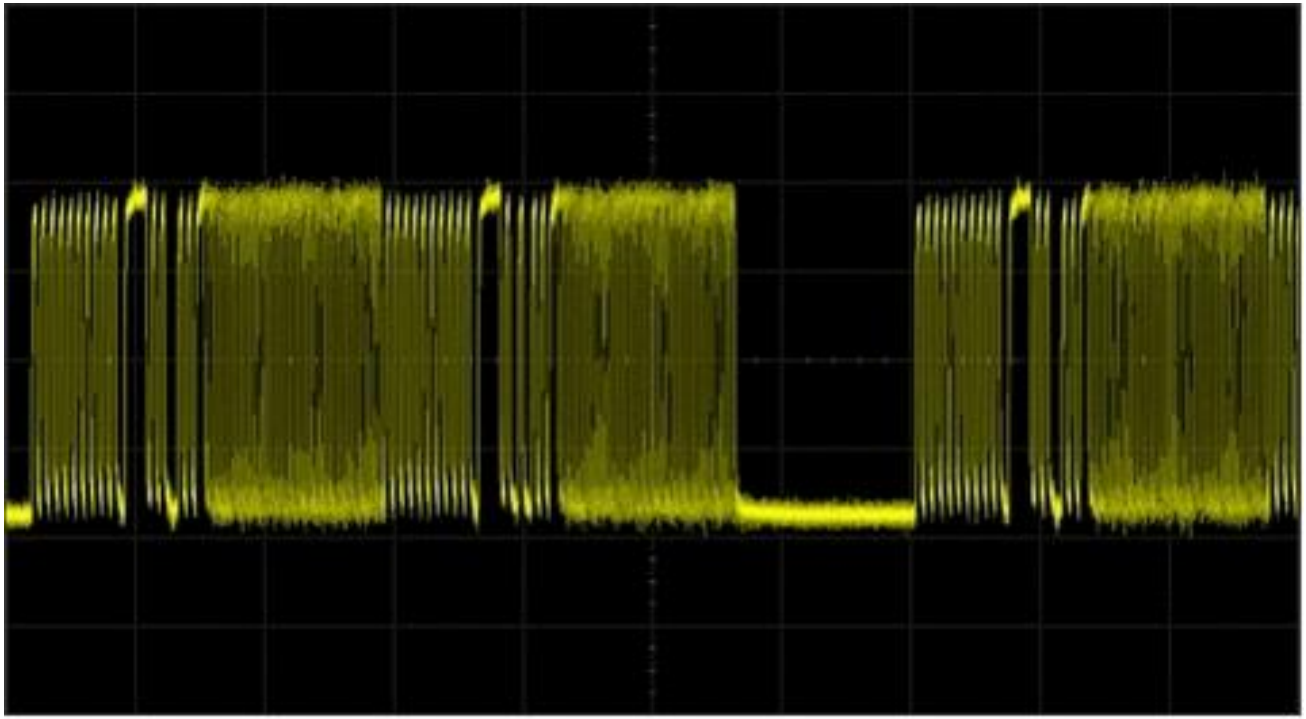


40 bits



PRBS (random gap)

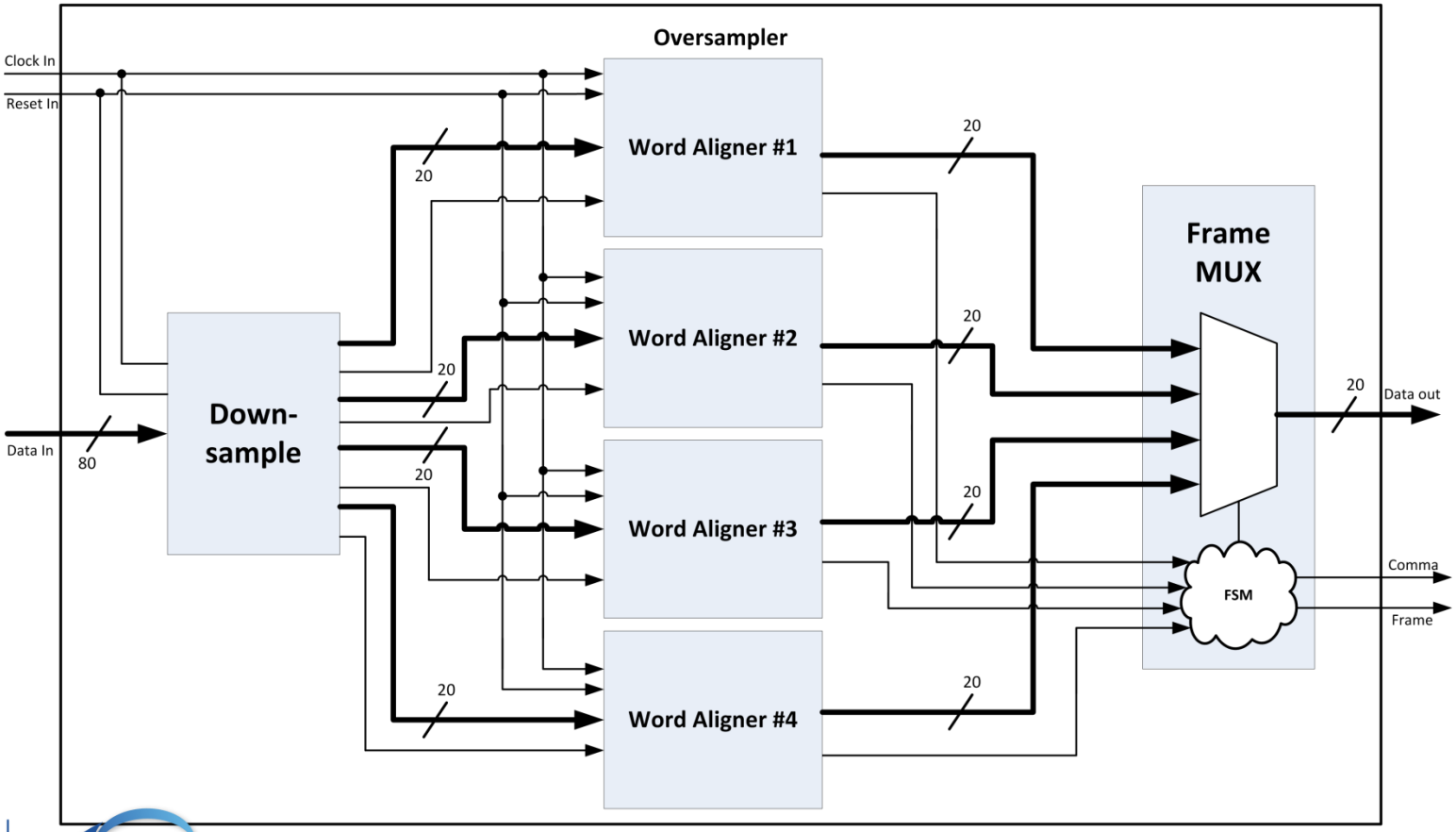
Blind Oversampler testing



PRBS (random gap)

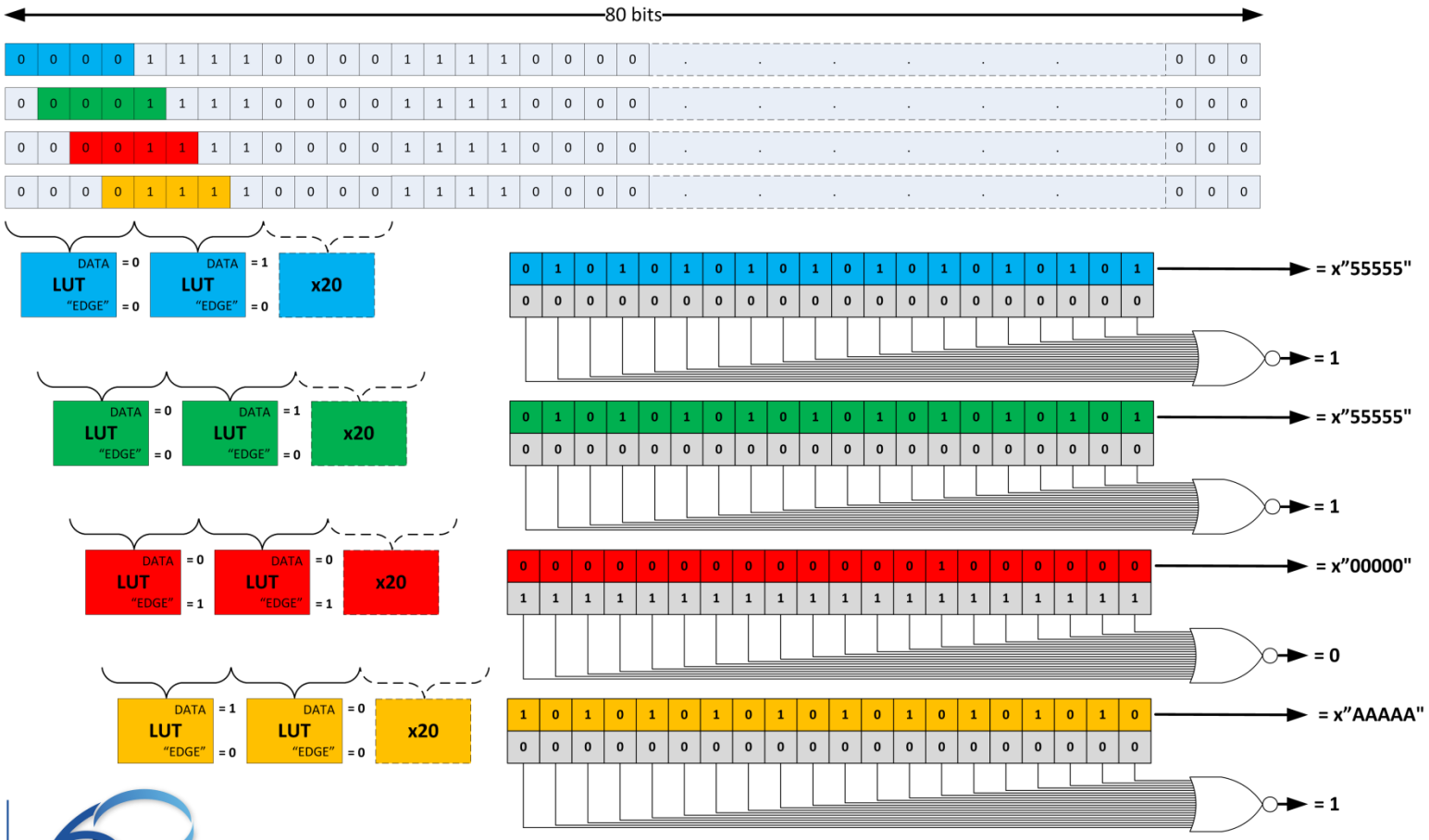
Upstream: Customizing the FTTH standard

Very fast fine phase alignment (block diagram)



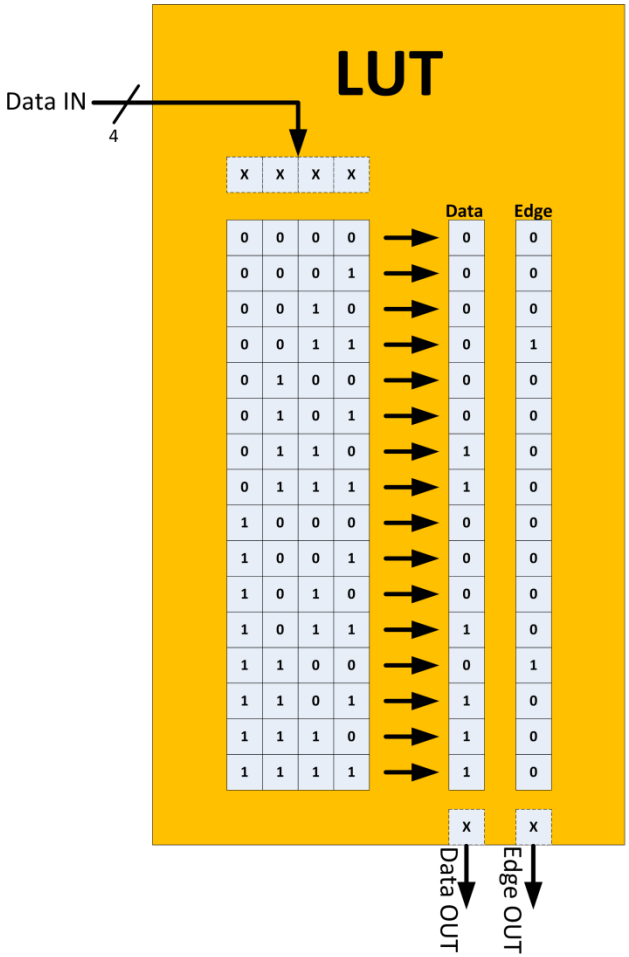
Upstream: Customizing the FTTH standard

Very fast fine phase alignment (more detailed)



VHDL design: Csaba Soos

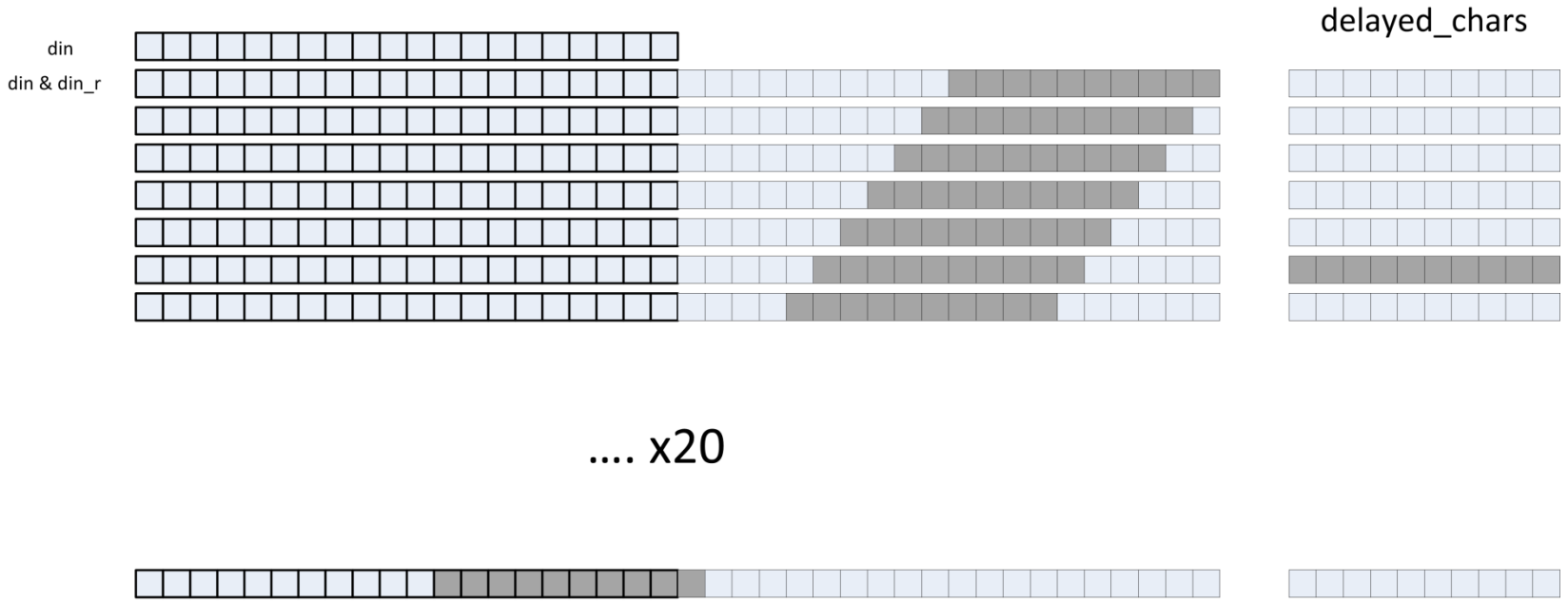
Look Up Table in detail



VHDL design: Csaba Soos

Upstream: Customizing the FTTH standard

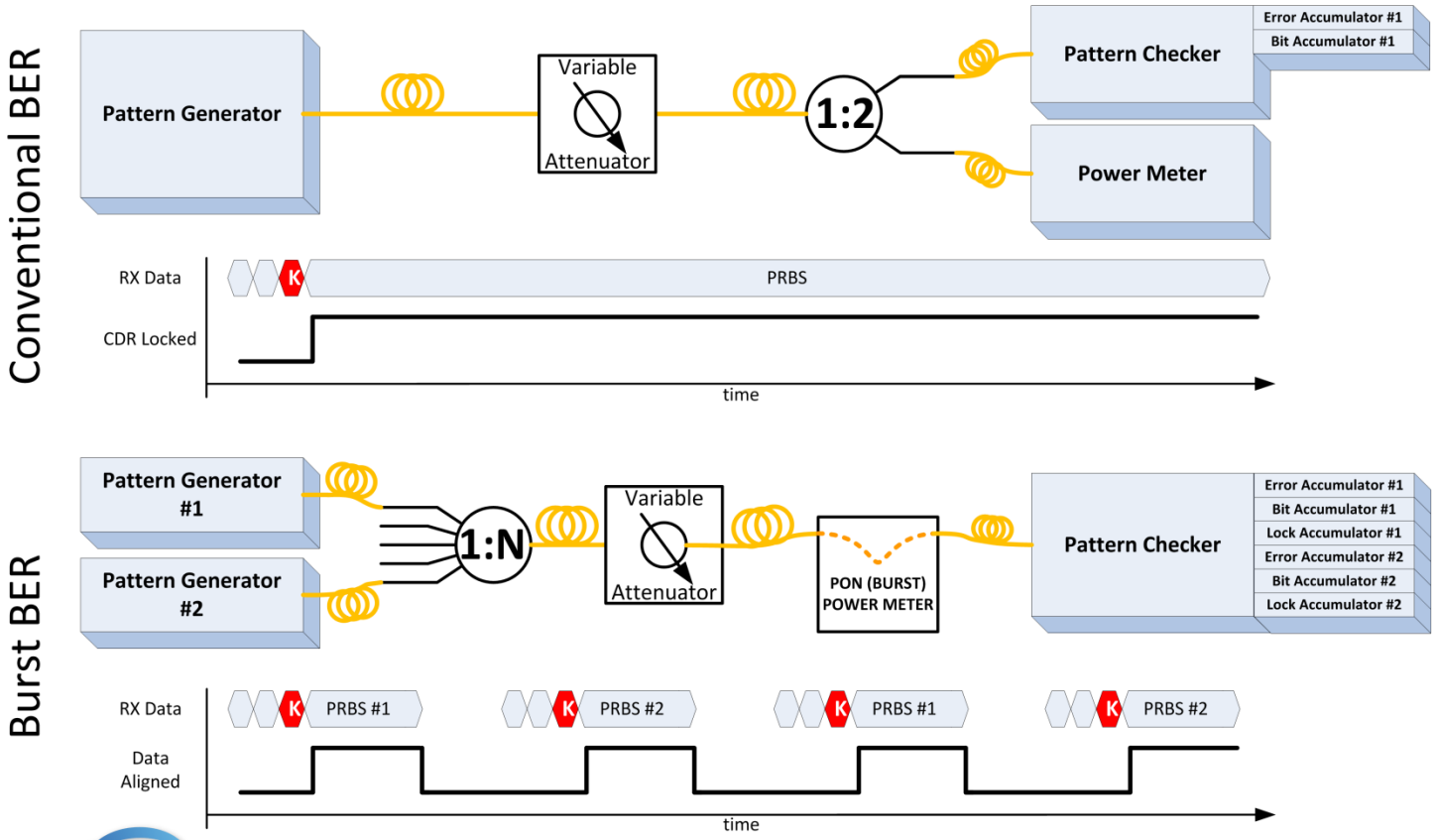
Very fast fine phase alignment



VHDL design: Csaba Soos

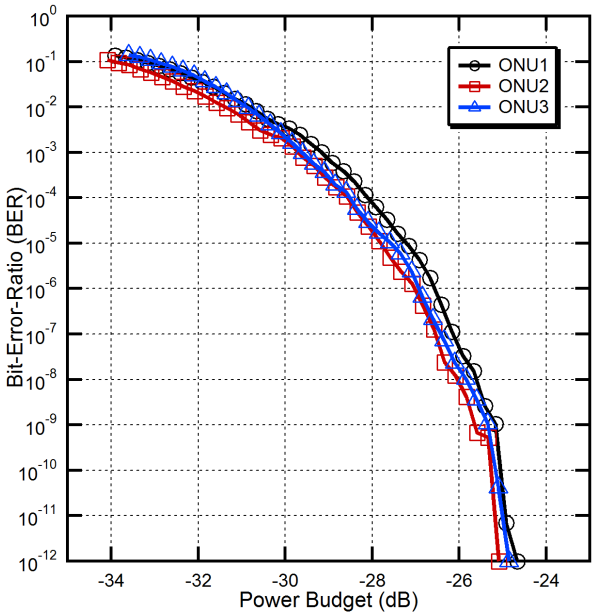
Upstream: Customizing the FTTH standard

BER vs BBER

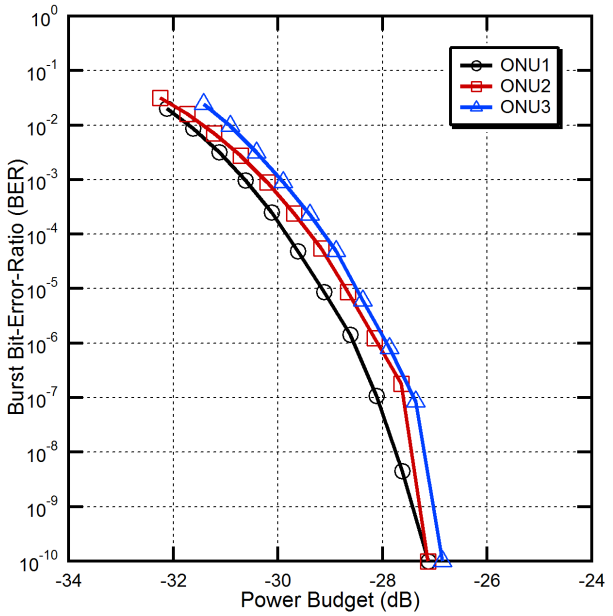


Results

Downstream path



Upstream path



Downstream path: ~25dB ➔ 1:128 splitting ratio
Upstream path: ~27dB ➔ 1:128 splitting ratio

5% unstable operation