Design of Low-Power, Low-Voltage, Differential I/O Links for High Energy Physics Applications

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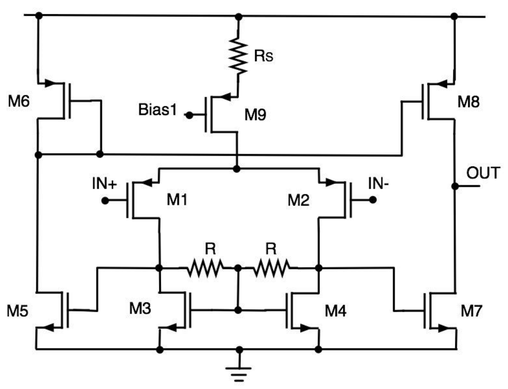
Abstract

High performance electronic links able to transmit data in the gigabits-per-second range will be key components in future high-energy physics tracking systems. Low-Voltage Differential Signaling (LVDS) is a well-known and widely used technique to provide a low-power, high-speed I/O interface for point-to-point transmission. Since the proposed link will be used in a harsh radiation environment, the design is based on core transistors only, with thin gate oxide and a voltage supply of 1.2 V. This value is not compatible with the nominal common-mode voltage of the LVDS standard, which is 1.25 V. Moreover, the very low power dissipation constraint forced us to reduce the differential swing. The driver has been designed for the output stage of the Strip Sensor ASIC (SSA) and Macro Pixel ASIC (MPA) of the so-called Pixel-Strip (PS) module designed for the CMS Tracker at HL-LHC. The SSA chip sends data to the MPA chip through a wire bonding interconnection, while the MPA, after its sparsification procedure, sends the data to the concentrator chip through the Service Hybrid. In the worst-case scenario, this link will have to drive a ~10 cm long, 100 Ω differential line. The link operates at 320 Mbps with 600 mV common-mode voltage and 100 mV differential swing. This design has been integrated in a 65 nm CMOS technology test chip and submitted for fabrication in September 2014

Receiver Circuit Design

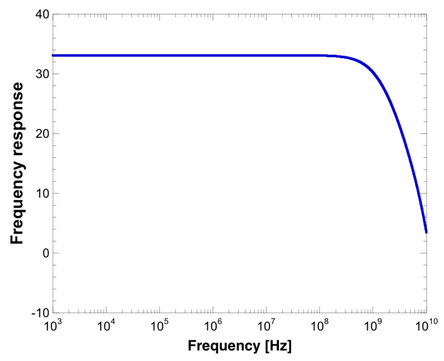
The receiver is a two stage amplifier. The first stage is a differential voltage amplifier with self-biased load. The second stage implements a push-pull structure.
The receiver is biased with 150 μA DC current. The GBP is about 12 GHz
The DC gain can be expressed as:

$$A_0 = 2 \cdot \frac{g_{m2}}{g_{ds4} + R^{-1}} \frac{g_{m7}}{g_{ds7} + g_{ds8}}$$



	TYP	Mean	σ
Positive transition delay [ps]	146.1	146.2	8.7
Negative transition delay [ps]	146.9	147.6	9.0
Duty-Cycle [%]	50.2	50.4	1.1
Total Power Consumption at 320Mbps [μW]	200	-	-
Bandwidth [MHz]	950	-	-
DC Gain [dB]	32	-	-

Mismatch analysis (500 runs) at 300 K

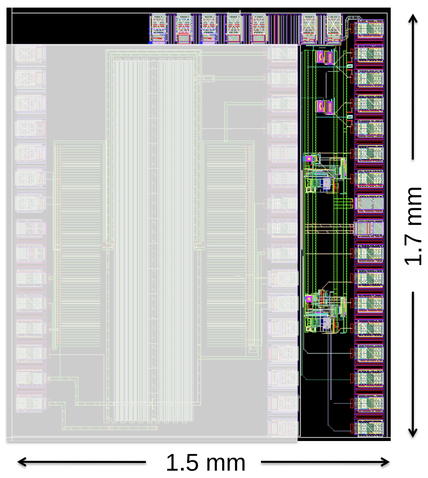


Prototype Chip

A first prototype is going to be submitted in the 65nm CMOS TSMC Technology. The chip includes:

- One conventional driver circuit
- One Slew-Controlled driver circuit with 4 selectable values of C_D
- Two receivers

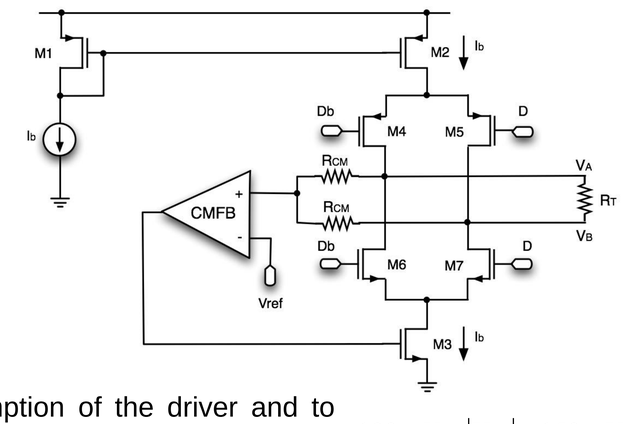
A few input pins are present to control the transmitter output current and the receiver DC biasing



Driver Circuit Design

➢ *Typical sLVDS driver circuit:*

- The bias current I_b is switched through the termination resistance according to the data input, and produces the correct differential output signal swing
- Typical LVDS drivers works well with 2.5V power supply since the voltage drop across the transistors consumes headroom with a 3.5 mA static current



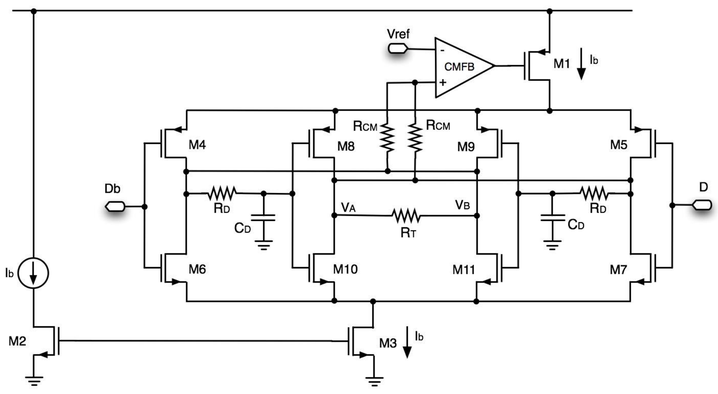
- In order to minimize the power consumption of the driver and to fulfill the requirement to design the circuit with core transistors only, the following differential output voltage and common-mode voltage at the transmitter output have been chose:

$$100mV \le |V_{OD}| \le 150mV$$
$$550mV \le V_{CM} \le 650mV$$

- At high data rate, an additional termination resistance is usually placed between the driver outputs to reduce the effects of reflected waveform returning to the driver due to imperfect termination and package parasitics
- This solution is not applicable here since it would double the power consumption (with the same differential output voltage value)
- The total power dissipation at 320Mbps is about 2.1 mW

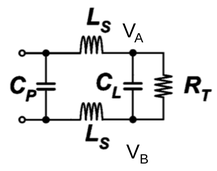
➢ *Slew-Controlled sLVDS driver circuit:*

- The slew-controlled driver (SCD) is based on [1, 2]. Part of the output current is provided by M8-M11 after a delay set with R_DC_D.
- The total power dissipation at 320Mbps is about 2.1 mW
- Both circuits implement the same Common-mode Feedback circuit (CMFB) based on a single-stage differential amplifier (A_0= 36 dB, f_{-3dB}= 8 kHz)

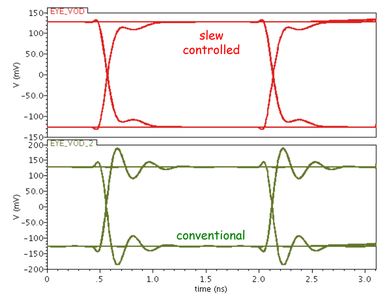


❑ *Simulation results:*

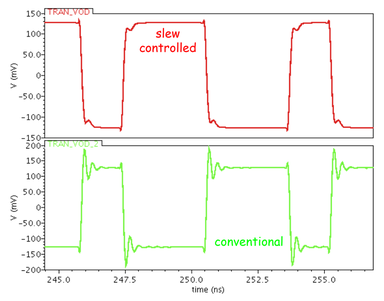
Package parasitics can be modeled with the following circuit:



C_P = 1 pF
C_L = 2 pF
L_S = 4 nH
R_T = 100 Ω



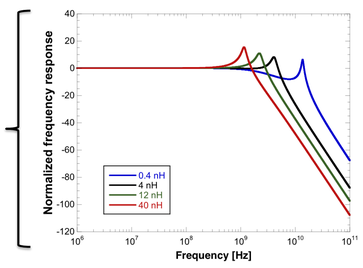
Eye diagram of the conventional and slew-controlled drivers at 640Mbps. Receiver not connected

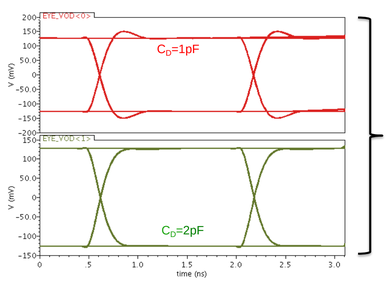


Transient simulation of the differential output voltage (V_A-V_B) for the conventional and the slew-controlled drivers at 640Mbps. Correct choice of R_D and C_D reduces the overshoot at the receiver input in SC architecture

❑ *Parasitic inductive component variations:*

Different values of the inductive component give rise to a different resonance peak



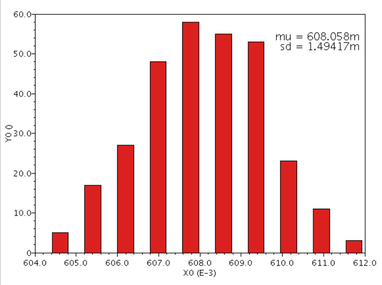


To cope with this effect, a SC driver with selectable values of C_D (0.5pF, 1pF, 2pF) has been designed

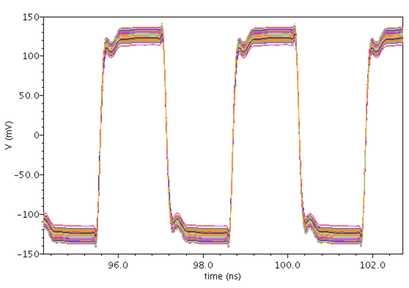
Normalized transfer function of the package parasitics model circuit for different values of the inductive component

Eye diagram of a slew-controlled driver for different values of C_D. The parasitic values are: C_P=1pF, C_L=2pF L_S=8nH

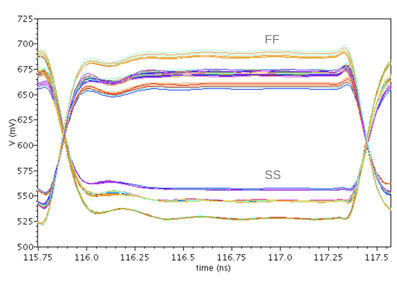
❑ *Monte Carlo and Four Corners simulation results:*



Monte Carlo simulation results of the common mode output voltage



Monte Carlo simulation results of the differential output voltage



Corner (TT, FF, SS, FS, SF) simulation results at different temperature values (-25°C, -10°C, 0°C, 27°C, 50°C, 75°C) of the differential output voltage

References

- [1] S. Jamasb et al., "*A 622MHz stand-alone LVDS driver pad in 0.18-μm CMOS*", Proc. IEEE Midwest Conf. Circuits and Systems (MWSCAS), 2001, Vol. 2, pp. 610-613.
- [2] A. Tajalli, Y. Leblebici, "*A Slew Controlled LVDS Output Driver Circuit in 0.18μm CMOS technology*", Journal of Solid State circuits, Vol. 44 (2), Feb. 2009, pp. 538-548.