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A Dedicated Front-end for Readout of Strip Detectors in the LHCb Upgrade Experiment

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Silicon strip detectors in the upgraded Tracker of LHCb experiment will require a new readout ASIC. It will extract and digitise analogue signals from the sensor, perform digital processing and transmit serial output data. The ASIC front-end comprises a charge preamplifier and a shaper. Fast shaping is required ($T_{peak} = 25ns$, fast recovery) to distinguish between the LHC bunch crossings.
A prototype of an 8-channel front-end was designed in CMOS 130 nm, fabricated and tested. The measurements showed very good performance. In particular, symmetrical output pulses with fast recovery times were observed.

Summary

The Large Hadron Collider beauty (LHCb) detector, operating at the Large Hadron Collider (LHC), has finished its Run I period, accumulating a large amount of valuable data. Despite its superb performance, it is clear that the LHCb experiment is statistically limited by readout electronics and data acquisition architecture, allowing it to collect data at the top rate of 1.1 MHz. The LHC machine is already capable of delivering more than one order of magnitude higher luminosity than presently used by the LHCb detector. This fact led the LHCb Collaboration to prepare a proposal of an upgrade of the LHCb spectrometer. One of the most important goals of the LHCb upgrade is the design of new front-end electronics allowing a full detector read-out at the bunch-crossing rate of 40 MHz˜.

A project of a common ASIC for the readout of silicon strip sensors in the LHCb Upgrade Tracker System, called SALT (Silicon ASIC for LHCb Tracking), has been started.
The ASIC will contain 128 readout channels, and be designed in CMOS 130˜nm. Every single channel will consist of a charge sensitive preamplifier, a shaper, and a 6-bit SAR ADC. The front-end and ADC blocks will be followed by digital data processing and fast data transmission.

The analogue front-end has to be very fast with a peaking time 25 ns and very short tail to minimise pile-up, and also have very low power consumption (1–2 mW/channel). It should have good signal to noise ratio (S/N>10), working with input signal of both polarities, for sensors capacitances between 5–35 pF. One of the main challenges for the front-end is to obtain a very short signal duration. The design goal was to verify whether a short symmetric pulse, with amplitude decreasing to 5\% after two peaking times, could be obtained with an acceptable shaper complexity and power consumption.
Preliminary studies showed that this is not possible with a standard semi-Gaussian shaping (with reasonable number of real poles in the transfer function), but that more complex shaping is required. Using complex poles helps but it is still not satisfactory. Theoretical calculations in Matlab, and Spice simulations showed that the required performance could be obtained by introducing both complex poles and zeros in the shaper transfer function.

A first 8-channel prototype of such a front-end was designed and fabricated in CMOS 130˜nm. Various measurements, comprising pulse shape, gain, noise, power consumption, were performed. The prototype was found fully functional confirming the simulation results. In particular, it was demonstrated that with a 3 stage shaper it is possible to obtain the requested pulse symmetry. The tests showed that the front-end works well in the 5–35˜pF range of input capacitance. Depending on biasing settings and sensor capacitance, the

front-end power consumption is between 0.8˜mW and 2˜mW. The obtained noise (ENC of about 1000 electrons for 10˜pF sensor) fulfills the specifications.

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