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First Results of the Belle II Silicon Vertex Detector Readout System

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At the heart of the Belle II experiment at KEK, there is a Vertex Detector composed of 2 layers of DEPFET pixels (PXD) and 4 layers of double-sided silicon strip detectors (SVD). The latter use APV25 front-end chips, originally developed for CMS, which are run in the so-called *multi-peak mode* that delivers several samples along the shaped waveform. Those are processed in the backend firmware to obtain precise amplitude and timing. The whole system (including the full DAQ chain) was successfully tested in a beam at DESY in January 2014 and first results are presented here.

Summary

In total, the future Belle II Silicon Vertex Detector (SVD) will comprise of 172 double-sided silicon sensors (entirely made from 6" wafers), being read out by 1748 APV25 chips. Those will be operated by floating low voltages with potentials at the respective bias voltages. In order to efficiently utilize existing power supplies from the previous Belle experiment (with a much smaller silicon detector), we will use radiation and magnetic field tolerant DC/DC converter modules developed at CERN (utilizing the FEAST chip).

Being a low-energy experiment, the dimensions are much smaller than at LHC experiments and thus the distance between APV25 chips and the back-end is just about 15 meters, which can be directly linked by copper cables without the requirements of intermediate repeaters nor optical links. The APV25 output signals, delivering a stream of switched analog levels at 40 MS/s, are refurbished in the back-end using Finite Impulse Response (FIR) filters implemented in FPGA firmware. These filters operate in real-time and are capable of removing the effects of both distortions due to frequency-dependent cable attenuation as well as reflections.

Not only digitization and signal conditioning will take place in the back-end FADC modules, but also signal processing, including strip data extraction, pedestal subtraction, a 2-pass common mode correction and zero suppression (sparsification). The APV25 chips will operate in the so-called *multi-peak mode* where several samples along the shaper output waveform can be retrieved. By default, six samples will be read out in Belle II. These data will be processed to find the particle timing with a precision of a few nanoseconds. Several lab and beam tests have been performed to demonstrate this powerful feature by offline data processing. In the future, we will implement such an algorithm in the FPGA firmware and simulations have already shown that this can be done with lookup tables providing sufficient precision. Thus, the predominant amount of off-time background hits can be discarded in order to reduce the overall occupancy and data rates.

Prototype modules of the complete hardware chain - from front-end modules to the DAQ - were built and operated in a beam at DESY in January 2014 together with the PXD. The geometry was made with realistic distances as to represent a sector of the final experiment. The electron beam energy was varied between 2 and 6 GeV and a magnetic field of up to 1T was utilized for some runs. The focus of this test was not so much on the sensor performance but rather on the full readout chain integrating both PXD and SVD for the first time as well as common aspects like tracking and Region-of-Interest (RoI) finding (where SVD tracks are extrapolated online onto the PXD planes to define RoIs in order to discard background data outside of those zones).

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