Contribution ID: **39** Type: **Poster**

A Generic Firmware Core to Drive the Front-End GBT-SCAs for the LHCb Ugprade

Tuesday, 23 September 2014 17:05 (1 minute)

The LHCb experiment has proposed an upgrade towards a full 40 MHz readout system in order to run between five and ten times its initial design luminosity. The entire Front-End electronics will be upgraded in order to cope with higher sub-detector occupancy, higher data rate and to work in a complete trigger-less fashion. In this paper, we describe a novel way to transmit slow control information to the Front-End electronics, by profiting from bidirectional optical connections and the GBT and GBT-SCA chipset capabilities. The implementation and preliminary validation tests are shown as well.

Summary

For the upgrade of the LHCb experiment, the entire readout architecture will need to be replaced in order to cope with higher sub-detector occupancy, higher rate and higher network load. In particular, the entire LHCb Front-End (FE) electronics will be upgraded to run in a trigger-less fashion, i.e. without the aid of a trigger, thus recording data continuously at the full LHC frequency, for a total data bandwidth of various TB/s.

Synchronicity across the whole detector will be maintained by a centralized timing and readout control system (TFC) by transmitting a set of commands and information to the whole readout system and by transmitting a deterministic and controlled clock. The TFC system is composed of a Readout Supervisor, which centrally generates the commands and it is interfaced to the LHC timing system, and a set of Interface Boards, whose main aim is to act as an active fan-in/fan-out with the rest of the readout system. The Interface Boards are also interfaced to the global LHCb Experiment Control System (ECS) via a PCIe interface bus on a host PC.

Thanks to the CERN development of the GBT chip-set and a fully bidirectional optical network with high bandwidth (2500 links at 5 Gb/s), it was proposed to merge the transmission of TFC information with ECS configuration and monitoring data at the FE: each FE will be interfaced to a Master GBT in order to receive fast commands and clock. On the same link, part of the bandwidth will be dedicated to ECS information which will reach the FE chips via the GBT-SCA. In order to drive the GBT-SCA chip correctly and transmit and receive ECS data properly, a generic firmware core has been developed. Such firmware runs on every Interface Board and it drives the GBT-SCAs in a generic way, covering almost all its functionality and supporting different implementations at the FE.

This is achieved by developing the firmware in a completely configurable way, i.e. the chosen SCA protocol can be selected in real-time via commands issued by the ECS system together with the configuration data and the destination of such data can be selected via a configurable mask. This firmware will allow driving generically the entire LHCb upgraded FE electronics over a total of 2500 optical links and about 90 Interface Boards. It is technology independent, developed in HDL language, it does not make us of any technology specific element and it is completely agnostic of the content of the data field. It is basically a generic SCA driver via optical links for the Back-End electronics.

The scope of this paper is to show the current implementation of the firmware. A first implementation in a test-bench is also being evaluated and results will be shown, validating the system. This system will play a crucial role while the development of the FE is ongoing in test-benches and lab tests.

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Session Classification: First Poster Session

Track Classification: Logic