A Patter Recognition Mezzanine based on Associative Memory and FPGA technology for L1 track triggering at HL-LHC

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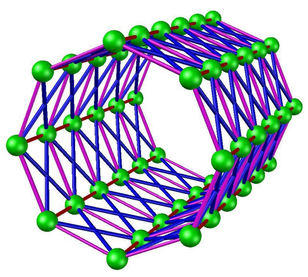
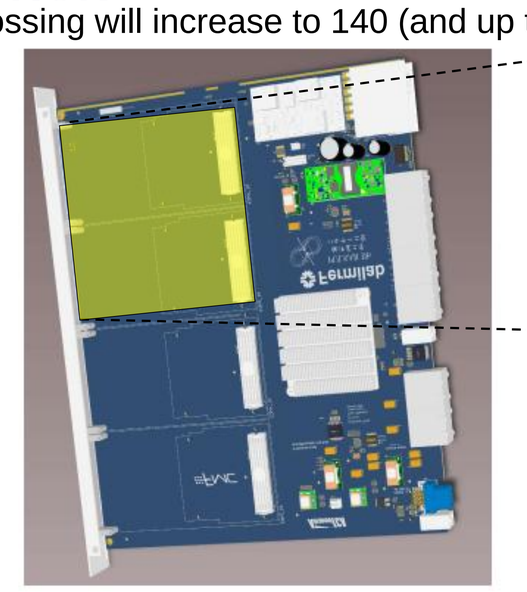
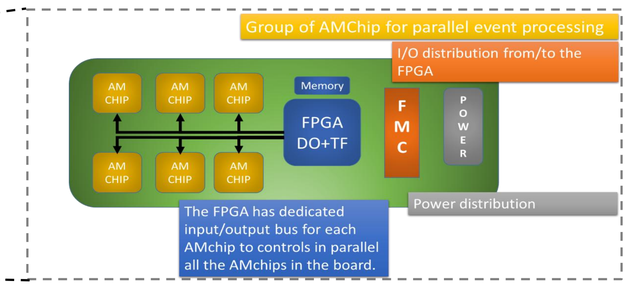
INTRODUCTION

At high luminosity LHC ($5 \cdot 10^{34}$ cm^{-2} s^{-1}), the number of interactions per bunch crossing will increase to 140 (and up to 200), and the trigger challenges due to the high pileup will be enormous.

- The silicon-based tracking information is the most effective way for pileup mitigation, if it can be made available to L1 trigger within the required latency (of a few microseconds).
- A dedicated hardware processor is hence the proposed solution to be used at L1 trigger to select interesting configurations at the 40 MHz bunch-crossing rate [1].
- The proposed CMS phase II L1 tracking trigger is conceptually organized in 48 trigger towers (6 η x 8 φ).
- Each tower is managed by a Advanced Telecom Computing Architecture (ATCA) crate. The basic card slot in each crate is the Pulsar II board[2] [J.Olsen Talk: "*Pulsar II: An FPGA-based Full Mesh ATCA Processor Board*".]



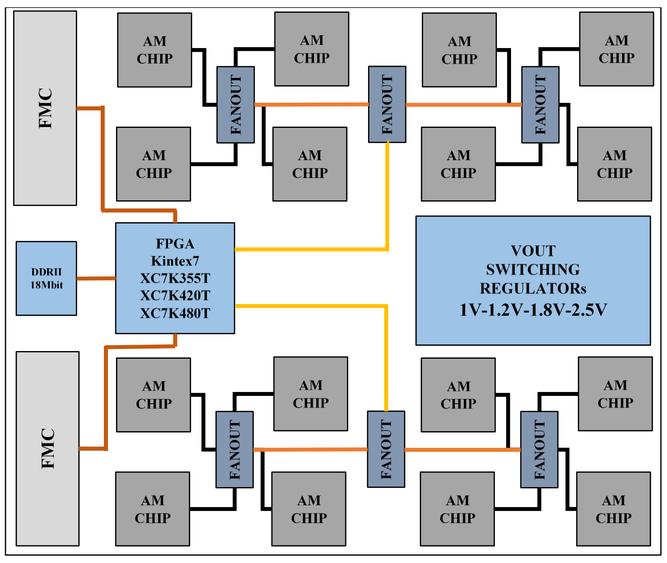




The Pattern Recognition Mezzanine (PRM), based on the Associative Memory and the FPGA technologies, is the mezzanine card to be hosted on Pulsar II mainboard to process the data.

PATTERN RECOGNITION MEZZANINE ARCHITECTURE

The Pattern Recognition Mezzanine (PRM) is a 14.9 x 14.9 cm^2 card hosting two High Pin Count connectors, a FPGA (XC7355T) and 16 AM chips. The FPGA will have the role of routing the hits coming from the tracker layers, collecting the candidate tracks and performing a track fitting operation.



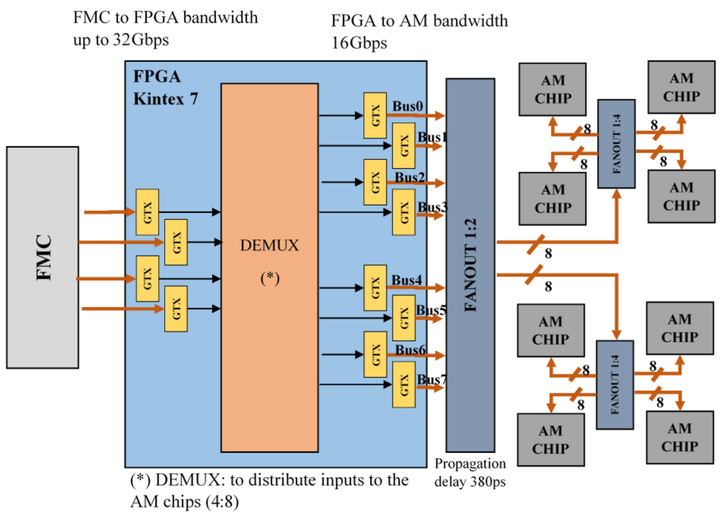
- Double FMC connectors
  - 14.9x14.9 cm2
- Kintex-7 FPGA
- I/O bandwidth (for each connector)
  - up to 64Gbps (24 GTX transceivers)
  - High speed LVDS
- AMchip05 & AMchip06 devices compatibility

The logic resources of the Pattern Recognition Mezzanine

- 16 Associative Memory Chips for a total amount of patterns:
  - PRM with AM05 → 4 kpatterns * 16 AM chips = 64 kpatterns/PRM
  - PRM with AM06 → 128 kpatterns * 16 AM chips = 2 Mpatterns/PRM
- FPGA devices supported

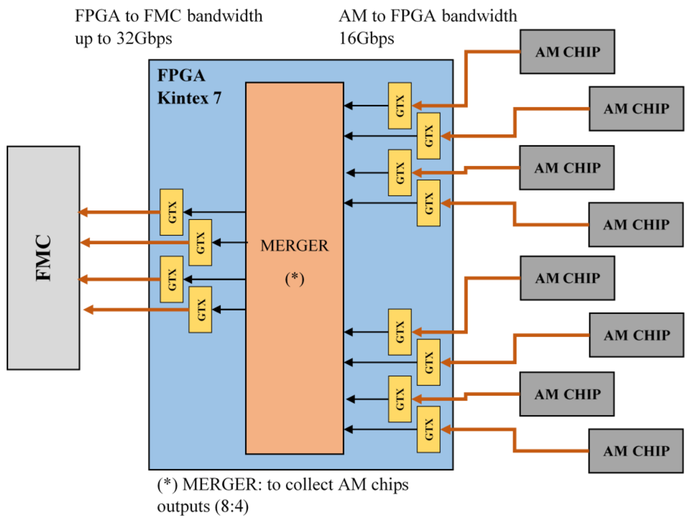
FPGA	Logic Cells	Memory Resource	GTX Transceiver	DSP
XC7K355T	356,160	25,740 Kbit	24	1,440
XC7K420T	416,960	30,060 Kbit	28	1,680
XC7K480T	477,760	34,380 Kbit	28	1,920

The data flow to distribute input hits to the Associative Memory Chips



- Dedicate transceiver for each input of AM chip bus
- 8 links @ 2 Gbps to AM chip
- Latency connections reduction:
  - Direct connection FPGA/AM chip
  - "fan-out buffer" (380ps)
- Total bandwidth (after the splitting) = 128Gbps
  - 8 buses x 8 AM chip @2Gbps

The data flow to collected output Roads from Associative Memory Chips



- A Road is the address of matching location
- Each output of AM chip is connected to FPGA (star connection)
- 8 links @ 2 Gbps connected to FPGA
- No bottleneck introduced by the FPGA device

EVENT TRACK RECONSTRUCTION

Pattern Matching (AM approach)

The Associative Memory has a modular architecture in which each chip includes both the memory required for storing candidate tracks (patterns) and the logic needed for the actual comparison.

- The device compares the SuperStrips ID (SSID) with all the stored patterns.
- The device returns the addresses (Road ID) of the matching locations.

Data Organizer (FPGA logic and memories)

The Data Organizer (DO) implements a Look-Up table containing the SuperStrip ID and the Road ID value according to the information written in the Associative Memory chip. It has two operation modes:

- **write mode:** the hits arrive in a random manner and are temporarily stored, until the event is processed, according to their SuperStrip ID;
- **read mode:** the hits that belong to the SuperStrip, considering the Road IDs calculated by the pattern matching, are sent to the track fitter stage.

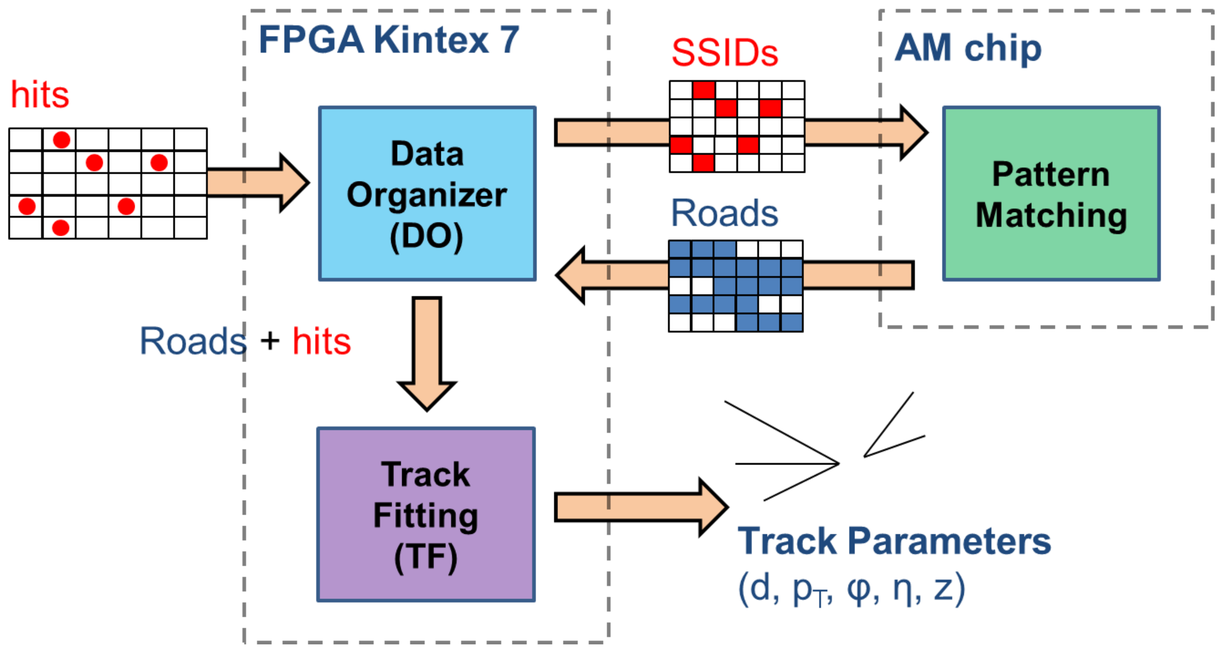
Track Fitting (FPGA logic)

A linear fit is done for each possible *track* computing all combinations of hits across layers. The fits are accepted or rejected according to their χ^2

- The resolution of the linear fit is close to that of the full helical fit in a narrow region (sector) of the detector
- The **FPGA DSP** resources are used to perform integer multiplication and addition operations.

$$p_i = \sum_{j=1}^{N} a_{ij} x_j + b_i$$

- p_i are helix parameters
- x_j are the coordinates in the silicon layer
- a_{ij} and b_j are constants from full simulation



CONCLUSION

The proposed processor for the L1 track trigger provides high computation power combining the Associative Memory and the FPGA technologies. It implements also the Data Organizer and Track Fitter stages to minimize the latency of the whole processing chain.

REFERENCE

[1] A. Annovi et al., *Associative Memory for L1 Track Triggering in LHC environment*, Nuclear Science, IEEE Transactions on, vol. 60, no. 5, pp. 3627–3632, Oct 2013

[2] J Olsen et al. *A full mesh ATCA-based general purpose data processing board,* 2014 JINST 9 C01041

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