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A Pattern Recognition Mezzanine Based on Associative Memory and FPGA Technology for L1 Track Triggering at HL-LHC

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The increase of luminosity at HL-LHC will require the introduction of tracker information at Level-1 trigger system for the experiments to maintain an acceptable trigger rate to select interesting events despite the one order of magnitude increase in the minimum bias interactions.
To extract in the required latency the track information a dedicated hardware has to be used. We propose a prototype system (Pattern Recognition Mezzanine) as core of pattern recognition and track fitting for HL-LHC experiments, combining the power of both Associative Memory custom ASIC and modern Field Programmable Gate Array (FPGA) devices.

Summary

With the increase of luminosity at 3×10ˆ34 cm−2 s−1, the number of minimum bias interactions per bunch crossing will increase up to about 400, causing an unmanageable increase in the rate of background if the threshold is not increased. The tracker information, more precise for track finding, is the key to solve this problem, if it could be processed in the required latency of few microseconds, too fast for the present implementation at higher trigger levels. A dedicated hardware processor is hence needed if tracker should be used at L1 to select interesting configurations at the 40 MHz bunch-crossing rate. Currently such class of processor is provided by the Associative Memory technology, already adopted in the CDF experiment and now in the ATLAS Level-2 trigger, the Fast Tracker processor where a longer latency (25 microseconds) is allowed.
We propose a processor, the Pattern Recognition Mezzanine, that combines the pattern recognition part using the new version of the Associative Memory device with the precise track fitting, performed by the last generation of FPGA devices, to send out the track information to the higher trigger levels within a shorter latency of few microseconds. This element will be the core of a trigger system where the I/O data distribution section plays also a crucial role. The best solution to this part of the problem lies in the ATCA standard. The PRM card will be hosted by an ATCM board, the Pulsar II developed for the CMS L1 tracking trigger demonstration.
The PRM is a 14.9x14.9 cm2 card hosting two FMC connectors designed to satisfy the VITA 57.1 standard specification, a Kintex FPGA (XC7355T) and 16 AM chips. The AM chips will be initially AM05, to test the functionalities, mainly of the Serial links, even if the number of patterns stored in each chip will be modest (5000), but it will also be compatible with the newer AM chip version (AM06) where the number of patterns per chip will be increased to 128000. The FPGA will have the role of routing the hits (time-multiplexing the events on chip subsets), collecting the candidate tracks, performing a track
fitting on them using different algorithms (PCA, Hough Transform, etc.) and then send out the results through the Pulsar board to the following trigger level. The FPGA position, very close to the AM chips, has been taken to reduce as much as possible the time needed for the Level-1 trigger decision and to integrate all the functionalities in one single board. An external low latency memory is added to increase the data storage capability of the device, in view of possible needs by the different fitting algorithms to be tested.
A mini FMC test-board has also been developed for configuration and standalone tests (no Pulsar or ATCA crate) to check the basic functionalities of the board, such as the GTX loopback to measure the bit error rate of the Serial Links.

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