Contribution ID: **31** Type: **Oral**

A 10 Gb/s Laser Driver in 130 nm CMOS Technology for High-energy Physics Applications

Thursday, 25 September 2014 11:35 (25 minutes)

The GigaBit Laser Driver (GBLD) is a key on-detector component of the GigaBit Transceiver (GBT) system on the transmitter side. As part of design efforts towards the upgrade of electrical components for the future LHC experiments, a 10 Gb/s GBLD (GBLD10) was developed in 130 nm CMOS technology. The GBLD10 is based on the distributed-amplifier architecture with pre-emphasis to achieve data rates up to 10 Gb/s and is capable of driving VCSELs with modulation currents up to 12 mA. The pre-emphasis function, to compensate for capacitive loads, is designed with the capacitive degeneration technique.

Summary

As an on-detector component of the GBT system for data transmission in High-energy Physics (HEP) applications, a GigaBit Laser Driver (GBLD) is needed operating at high data rates and displaying radiation tolerance. Although a 5 Gb/s GBLD has been demonstrated, a GBLD with 10 Gb/s data rate is desired for some detector systems. In this paper, we present a 10 Gb/s laser driver IC (GBLD10) implemented in 130 nm standard CMOS technology. The GBLD10 employs a novel distributed-amplifier architecture with pre-emphasis to achieve 10 Gb/s while keeping the power consumption low. In the proposed distributed architecture, the modulation stage and pre-emphasis stage of the laser driver are distributed over five uniform stages. To achieve the wide-bandwidth operation, T-type differential artificial transmission lines are carefully designed between the stages to absorb the parasitic capacitance. Three-terminal inductors with area of 130 µm x 130 µm each are chosen to implement the artificial transmission lines to save silicon area. The pre-emphasis function is an important feature of the GBLD to compensate for the performance degradation due to the external capacitive load. In this design, the pre-emphasis is realized by creating suitable zero and poles in frequency domain for emphasis amplitude control. Capacitive source degeneration approach is deployed to implement the zero and poles needed. Multiple DACs are used to program the different amplitudes independently to adapt to different VCSEL devices characteristics. The modulation current can be programmable from 0 to 12 mA by a 6-bit DAC while the pre-emphasis current can be programmable from 0 to 6 mA by a 4-bit DAC. The laser bias current can be set between 2 to 43 mA by an 8-bit DAC. These DACs are controlled via an I2C digital interface. The chip is powered by a single 2.5 V power supply. An on-chip voltage regulator generates the 1.5 V supply voltage for the core digital circuits. The total die size is 2 mm x 2 mm. The GBLD10 prototype chip design has been submitted for fabrication in February, 2014. It is going to be packaged in a 4 x 4 mm2 QFN24 plastic package. The chip measurement will be carried out in the summer of 2014 and the measurement results are expected to be presented at the TWEPP conference.

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Session Classification: ASICs

Track Classification: ASICs