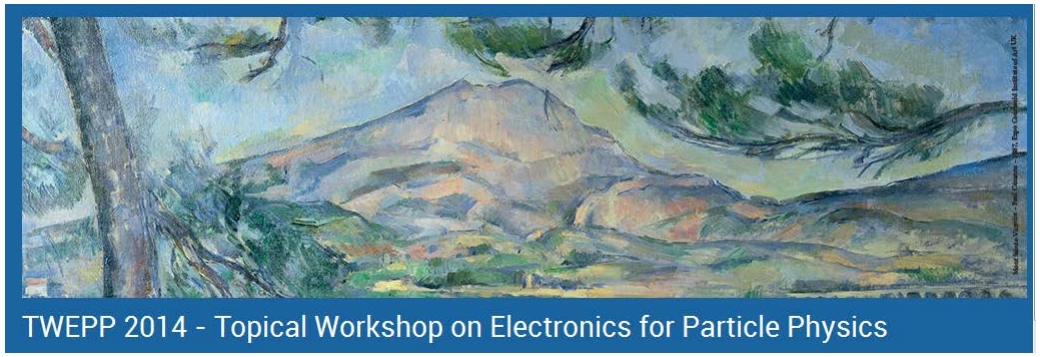


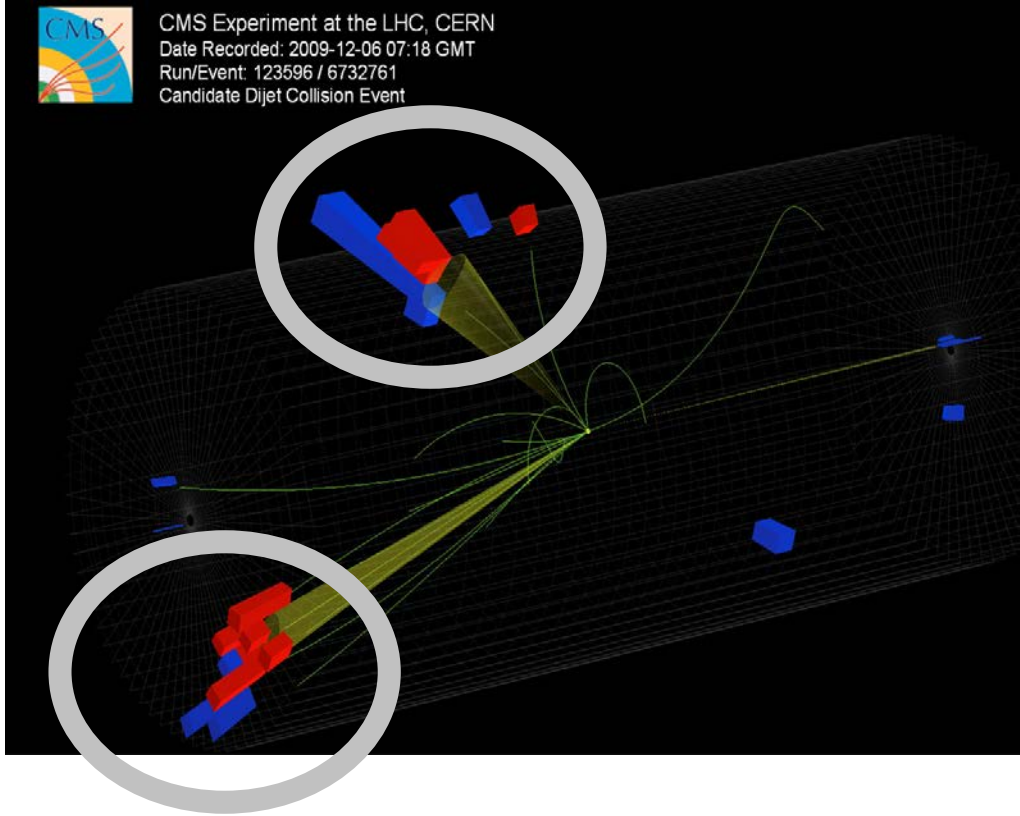
Technological Prototype of a Silicon-tungsten Imaging Electromagnetic Calorimeter.

R. Cornat, on behalf of the CALICE collaboration
remi.cornat@in2p3.fr

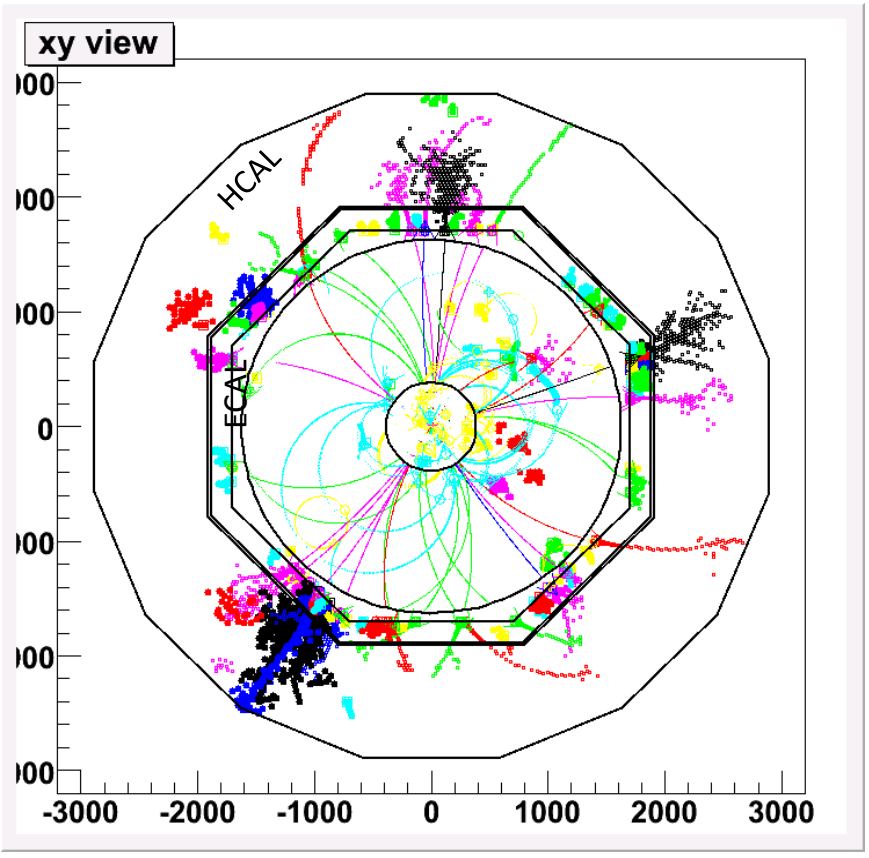
Grant ANR-2010-0429-01

Highly granular calorimetry

From this...



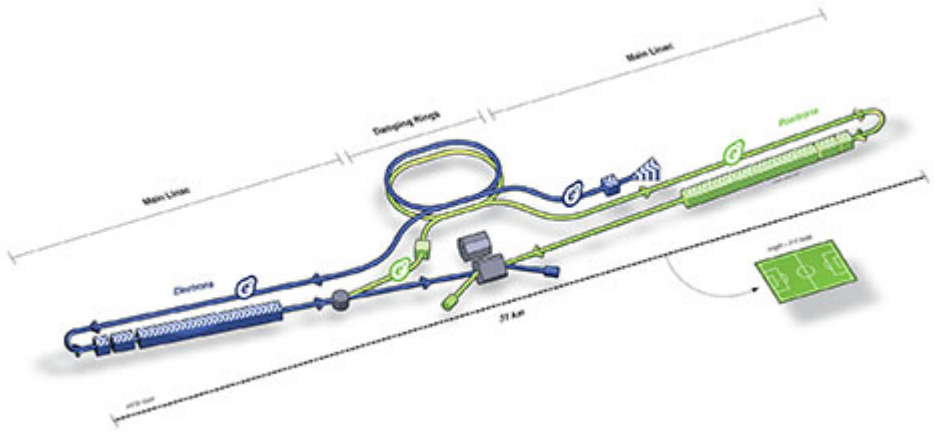
to this :

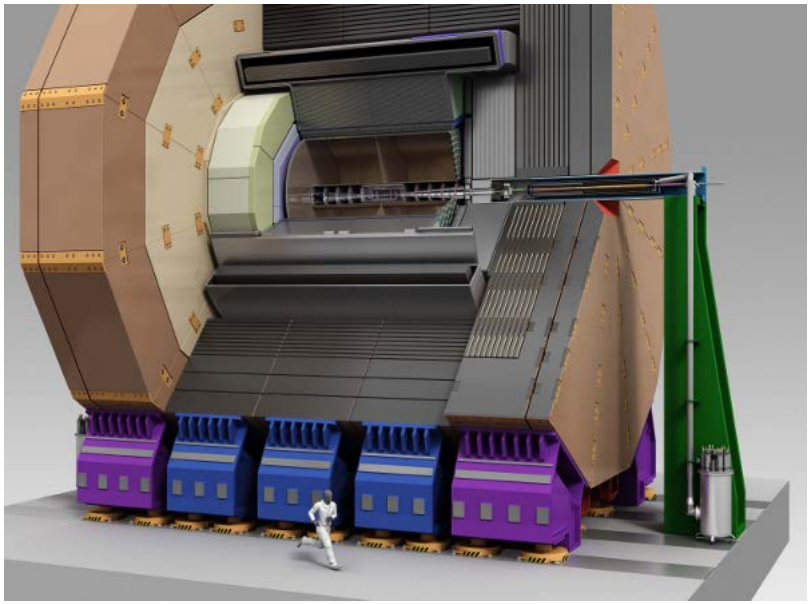


A mix of technologies qualified with prototypes achieving

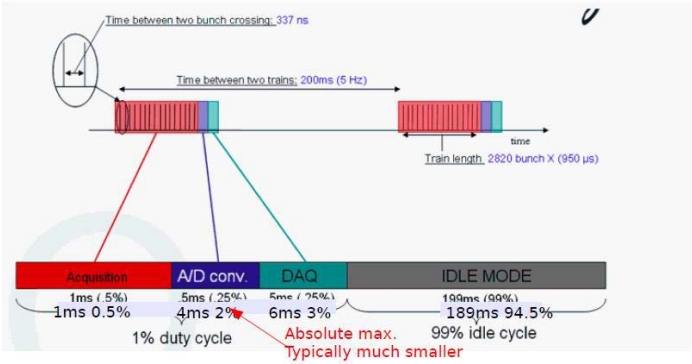
5000 “calorimeter grade” channels/dm^3

ILD concept





Large radius and length for a good separation of particles, large (4 T)magnetic field and calorimeters inside the coil.



Bunch trains @ 5 Hz allow for powering at 1-2% duty cycle. This has a strong impact on overall design : passive cooling, low data rates, daisy chained boards…

Time line

Proof of concept

- Linearity
- Resolution
- Sensors
- Very front-end

1500 channels/dm^3

Feasibility of design options

- Compactness
- Granularity
- Front-end
- Power pulsing
- 2m Long SLAB

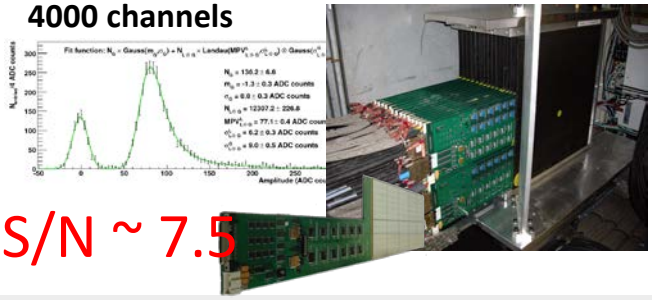
V1 : 4000 channels/dm^3
V2 : 5000 channels/dm^3

Construction

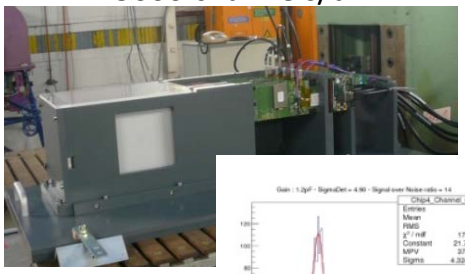
- Integration
- Environement
- Services
- Industrialization
- Tooling
- Project org.

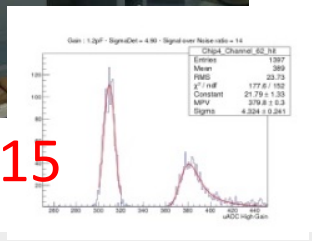
...10000 channels/dm^3

2004-2008
30 layers
4000 channels



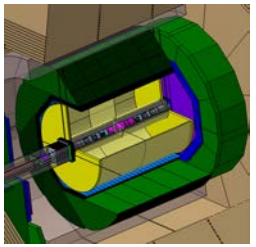
S/N ~ 7.5



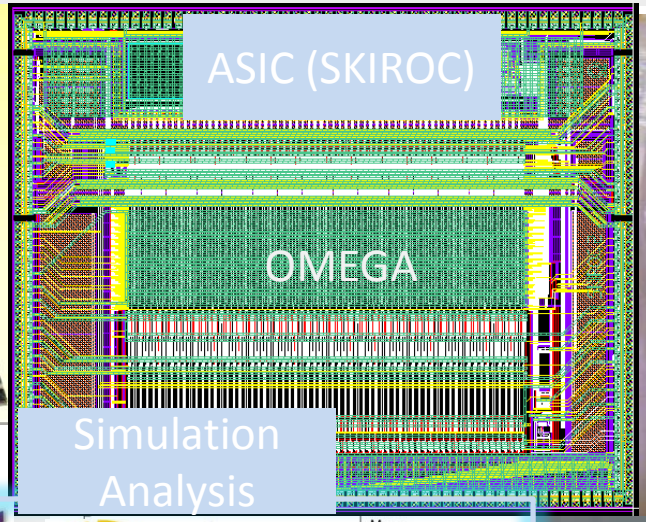


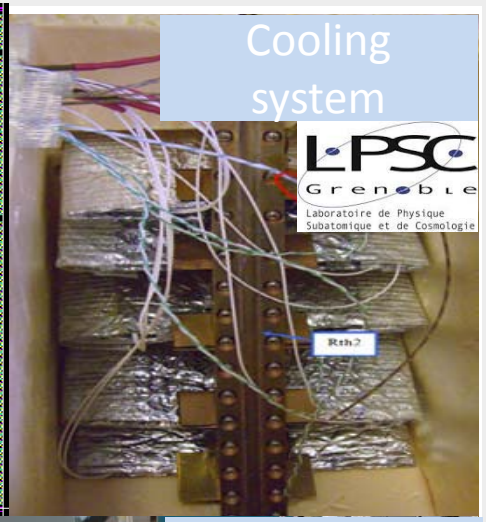
S/N ~ 15

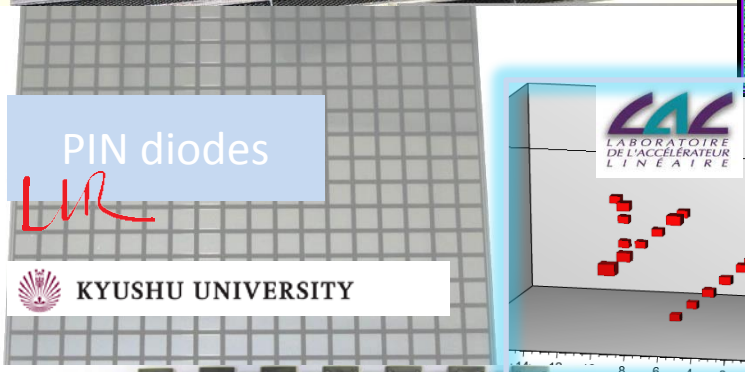
~24 X0, 20 cm thick
~2500 m^2 active detectors
~100M readout channels

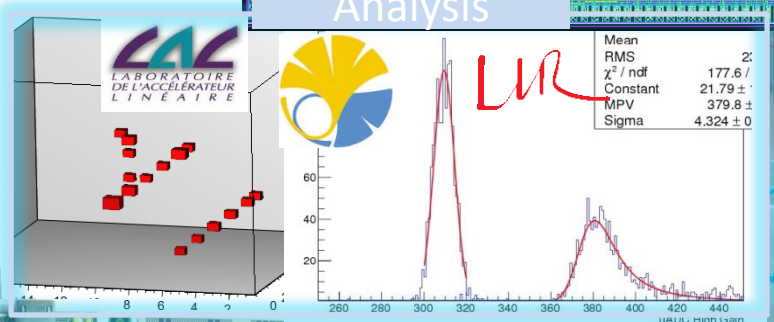


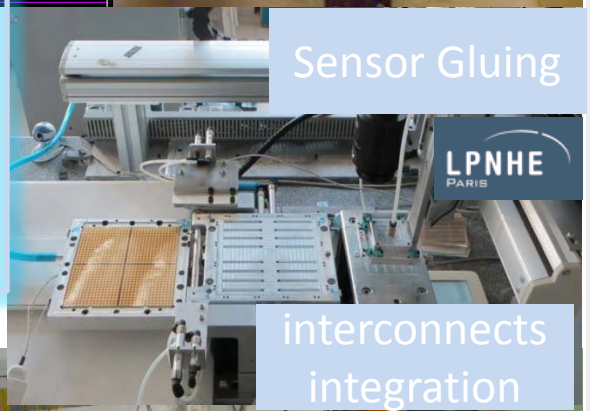
Prototyping : who is doing what

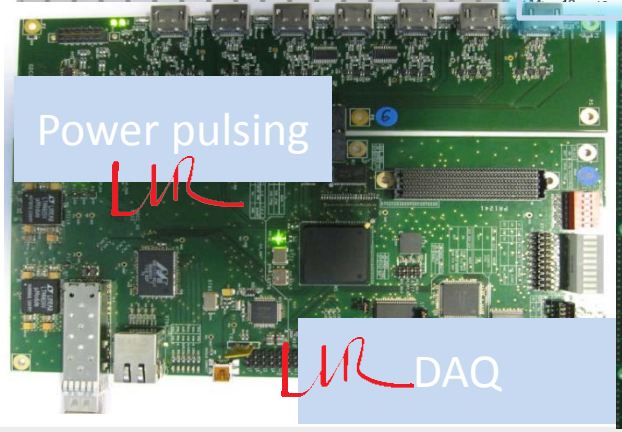


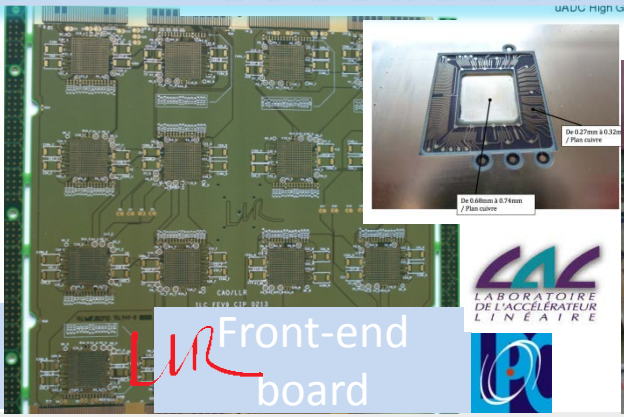


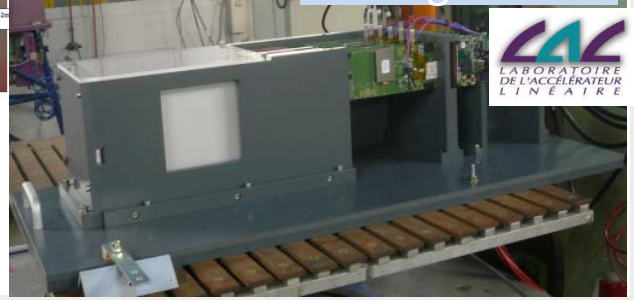




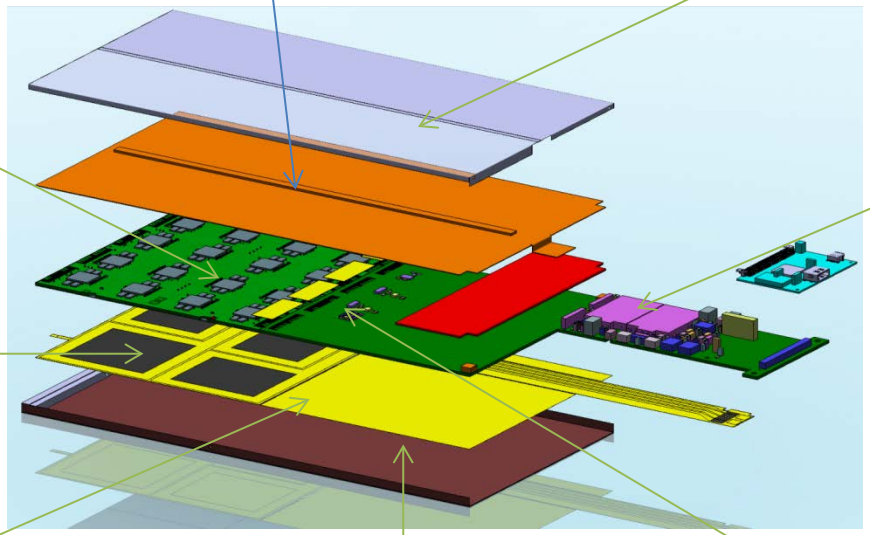








A detector module



Coper sheet for cooling

Cover (EMI shielding)

PCB 1024 chn. 16x skiroc2

Power pulsing circuitry (400 mF)

Si PIN diodes

Front-end, DAQ, TFC Not shown

HV kapton

A “short SLAB”

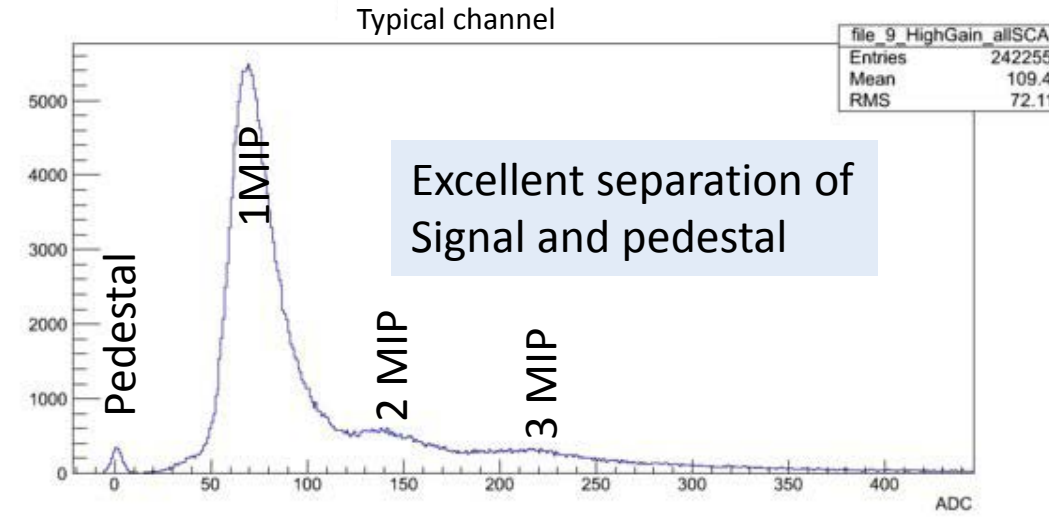
Stiffener, Absorber Carbon fiber + W

FCC Interconnects

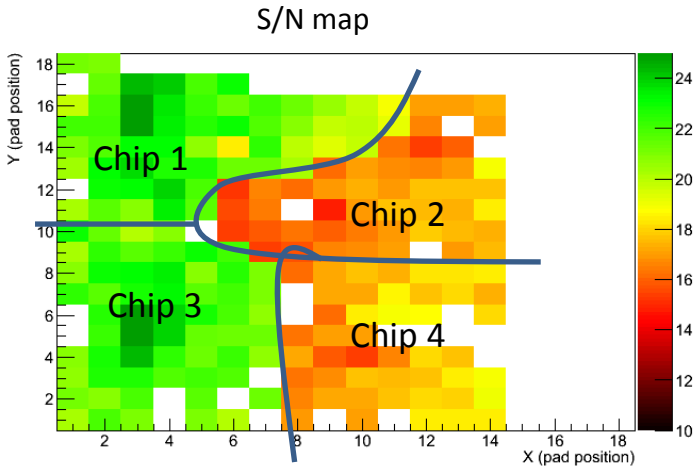
A first version

Up to 8 layers in test beam (12 build) with 213 channels each

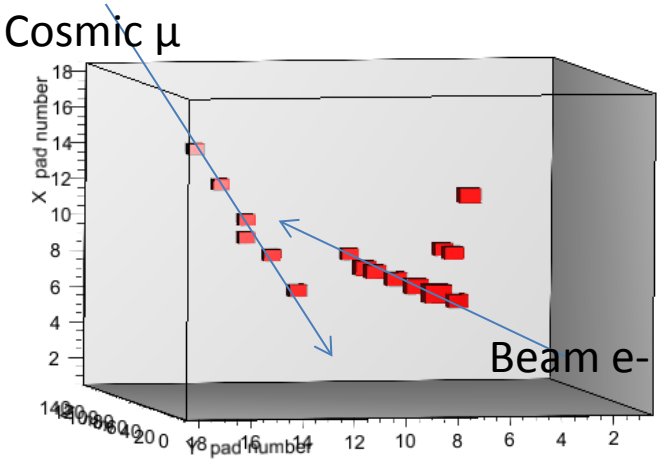
Low energy (<6GeV e-) test beams @DESY



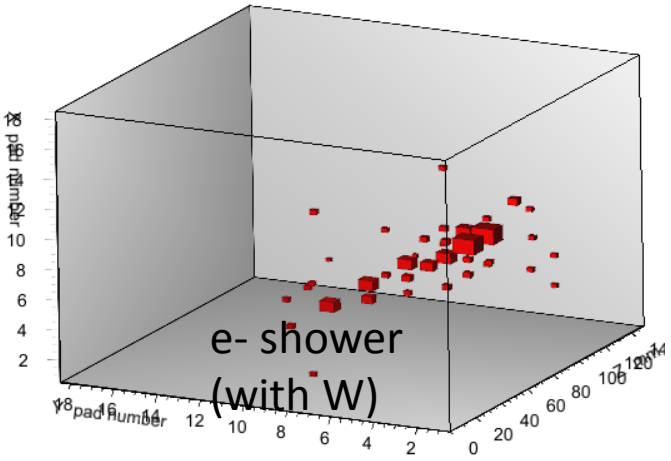
Excellent separation of Signal and pedestal



S/N better than the target (10), non uniformity understood (pixel-pcb capacitance)
EMI (chip 2 and 4 close to digital lines) and PSRR can be optimized (multi-trigger events)



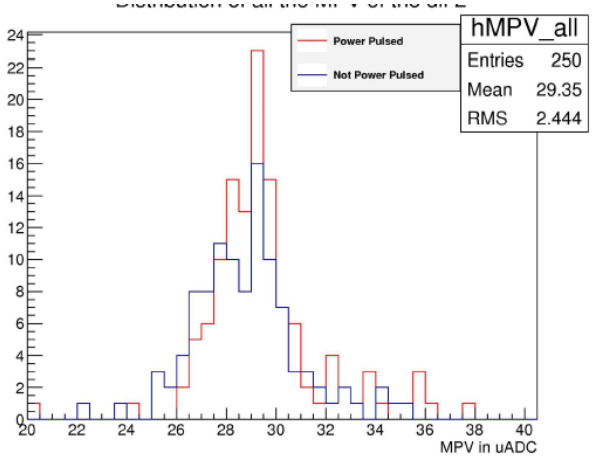
6 detector SLABS
1278 channels
10% off due to out-of-range calib.



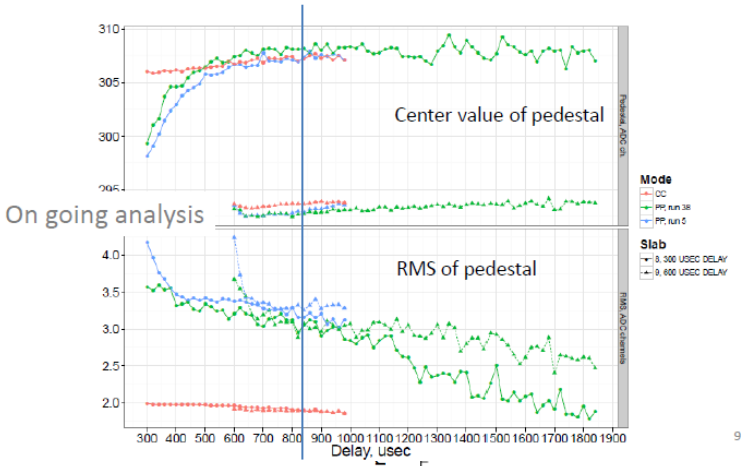
Chips in power pulsing mode

Principle : V remains constant while I varies, expected power-on time O(50µs)
Here : pulses of 1.2 A per board (>10A per complete module) @5Hz, 1% duty cycle

At system level, no significant effect observed on noise, pedestal, MIP value but effective power-on time is O(1ms) (=plateau reached for pedestal value)

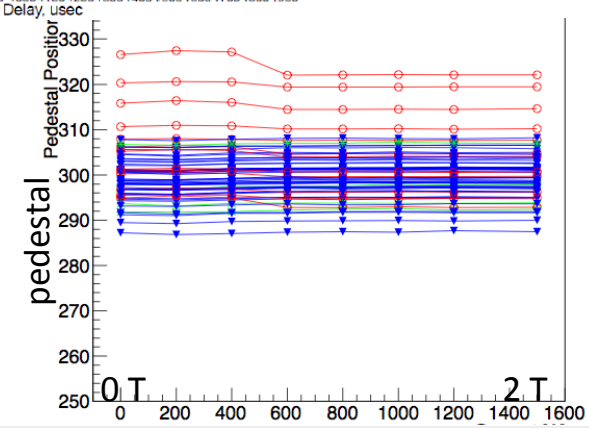


MIP in ADC units with power pulsing or without

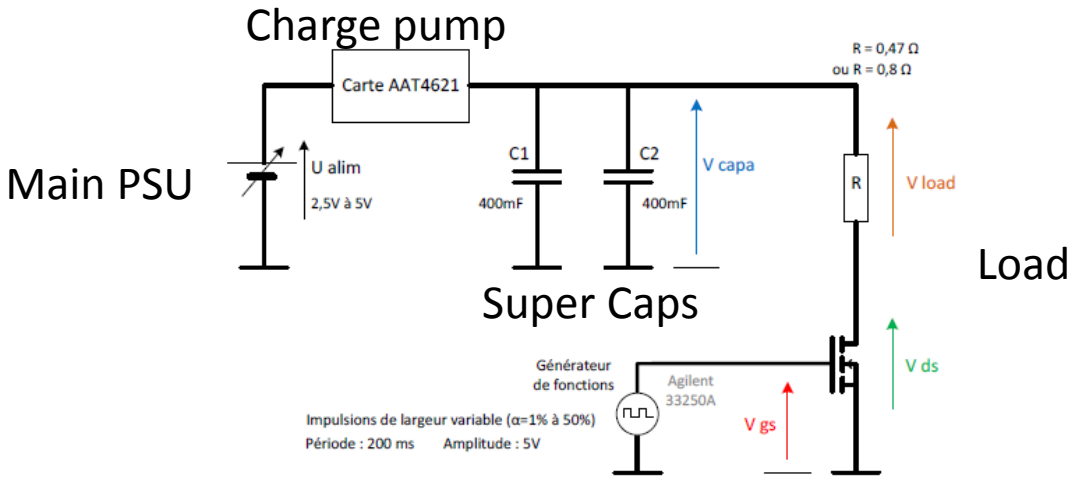


On going analysis

Tested OK in magnetic Field up to 2T

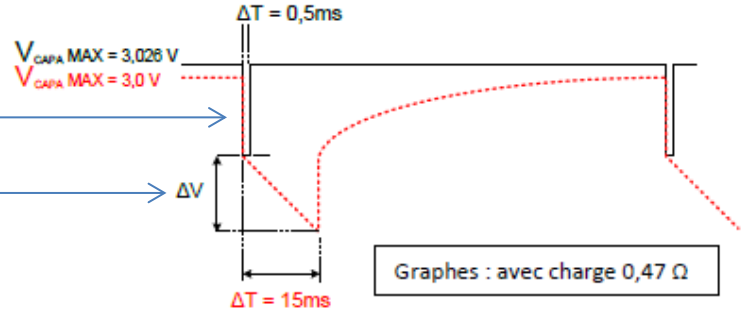


Power pulsing



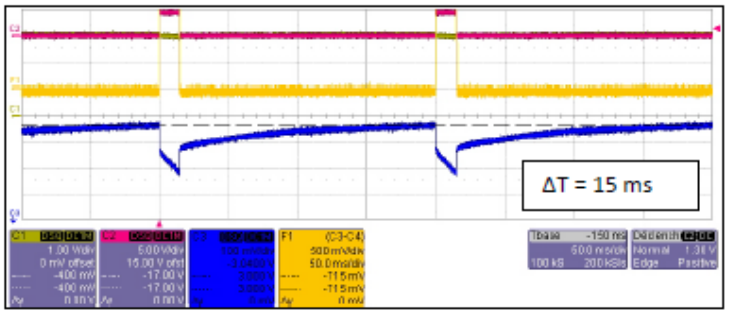
ESR (16 mΩ)

Constant current discharge



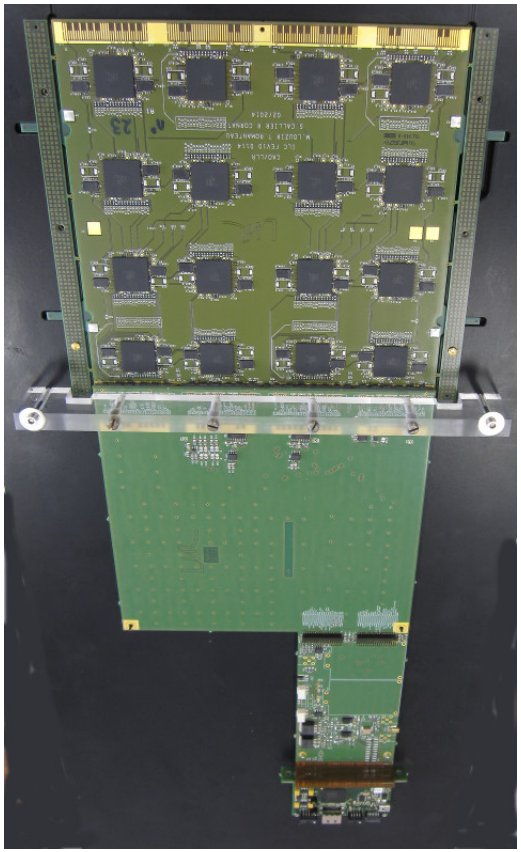
12A pulses, 31mV drop @1% Duty cycle (5 Hz)
124 mA mean current

10 000 channels could be powered with 2 AA battery cells for 24h

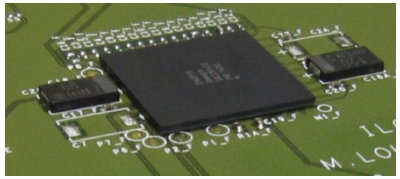


Next version(s) of VFE board

18 x 18 cm^2 front-end board includes 1024 channels (16 chips),
almost perfect flatness required for gluing the sensors : 1.6mm symmetrical stacking



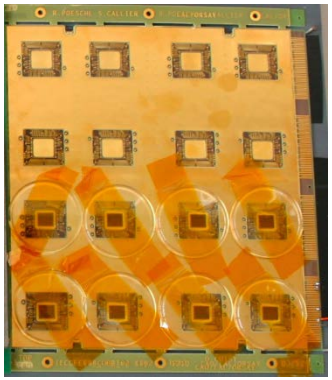
LFBGA packaged chips
and Panasonic Sp-CAP CX series
⇨ 1.1mm thick components envelop



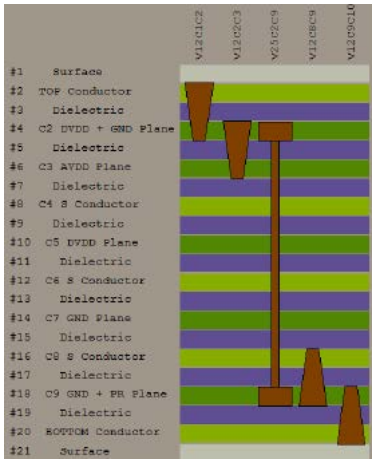
With packaged chips version the overall module thickness would be 5.5 mm (+absorber) : >4600 ch/dm^3

Naked die version would provide optimal module thickness (<4mm in total, >6000 chn/dm^3)

Electrical tests are ok but flatness is incompatible with sensor gluing.



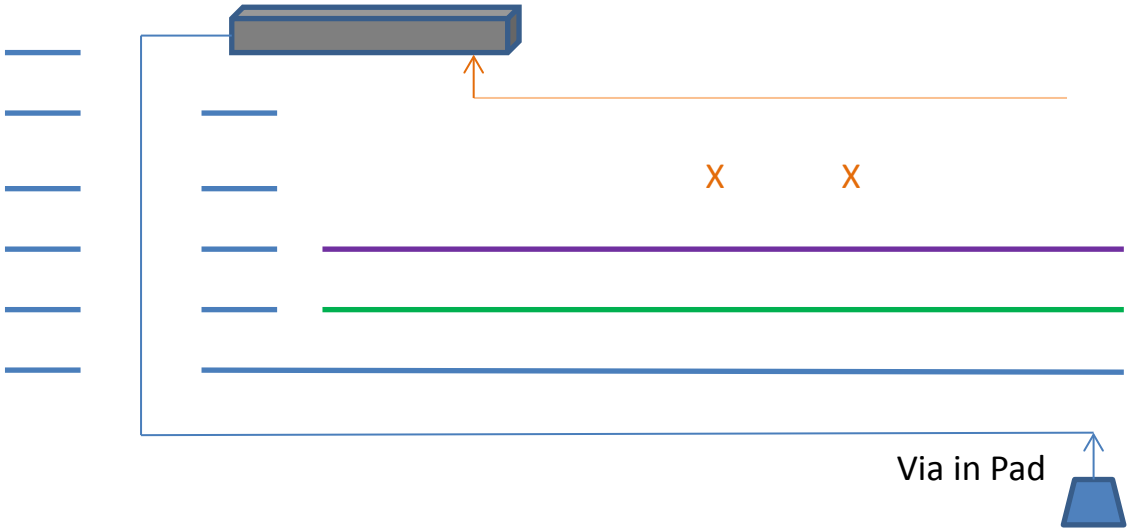
VFE board



Symmetric stack will improve flatness (100 µm deviation from perfect plan), required for wafer gluing

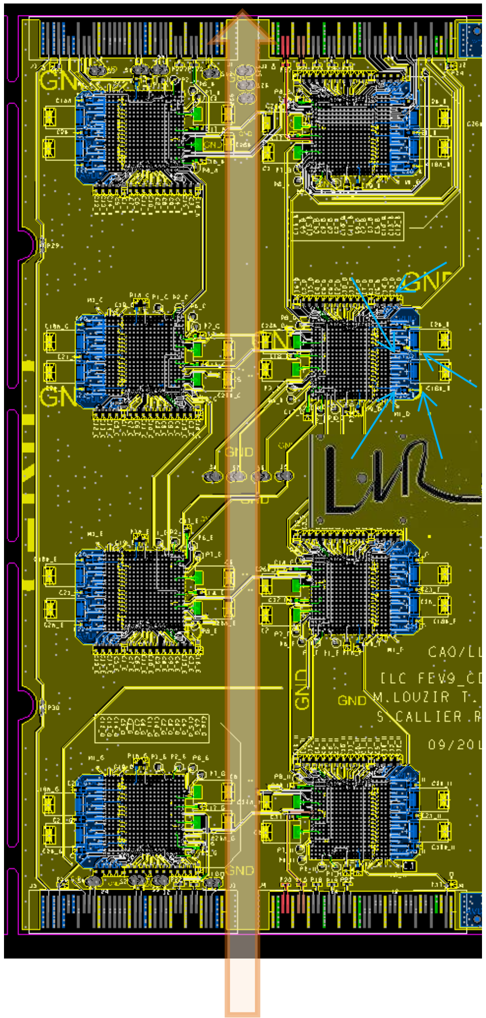
Analogue signals shielded with AVDD

Digital traces shielded with GND and kept away of analogue (as much as possible)

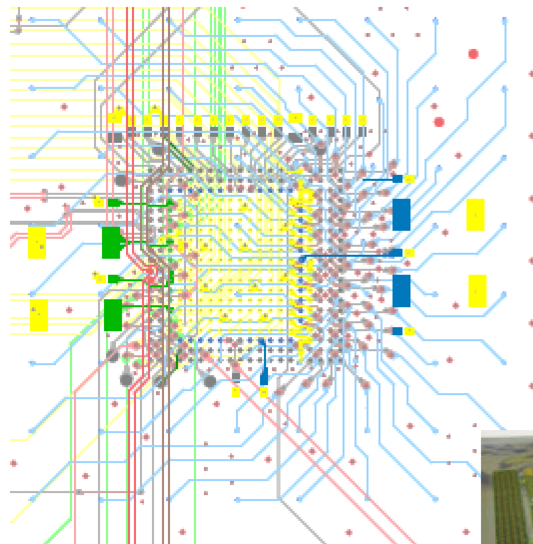


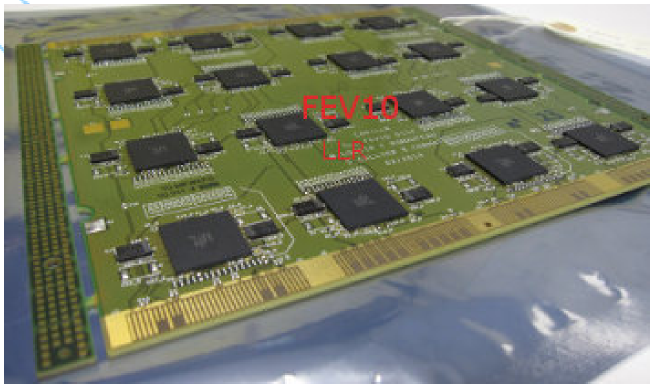
VEF board : routing

Half board shown



Detector channels →
routed on lower layers, uniform pattern





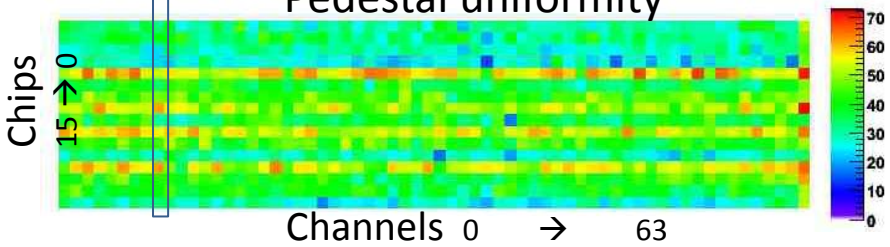
Path for digital signals
on upper layers, due to low occupancy daisy chain and openc collector are possible

Electrical tests (packaged chips)

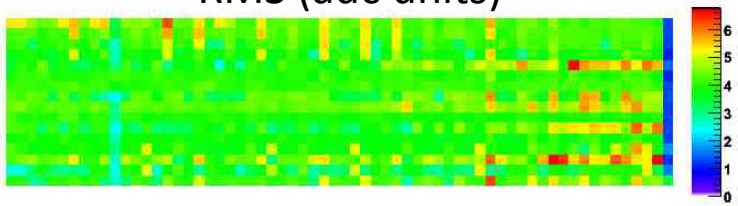
Board is tested without sensors : preamplifiers may not be biased properly,
All tests made with power pulsing at 2% duty cycle and 1 ms power-on time

With only **one** channel per chip allowed for triggering (avoids internal digital noise due to triggers) considering a MIP at 75 adc units (MPV), S/N is expected to be better than 15.

Pedestal uniformity



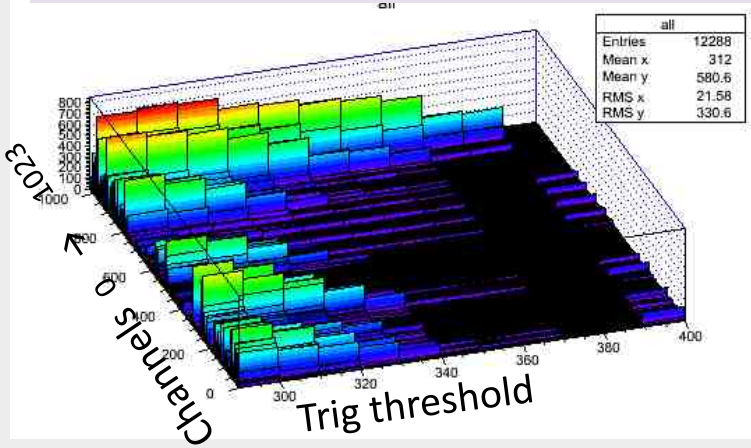
RMS (adc units)

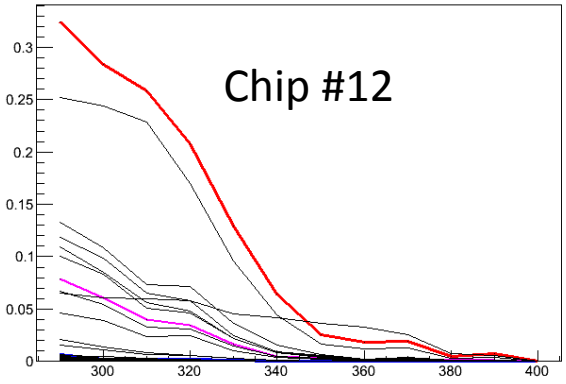


Enabling **all** channels for triggering, pedestal RMS is ~doubled.
Known sensitivity of the chip against triggers switching noise & PSRR

New chip version 2b and new prototype in SOI XFAB 0.18 should improve this

Noise erf() curves (aka. S curves) : % noise triggers w.r.t. trigger threshold (normalized)



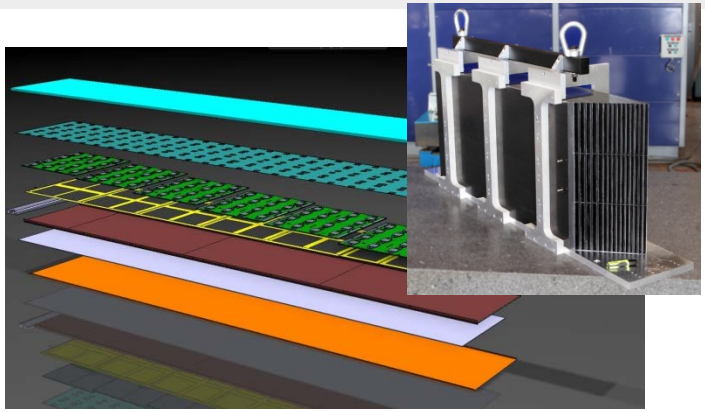


Disparity not understood
According to our calibration procedure 15% of the channels would be switched off. (10% acceptable for φ)

Toward a full length module

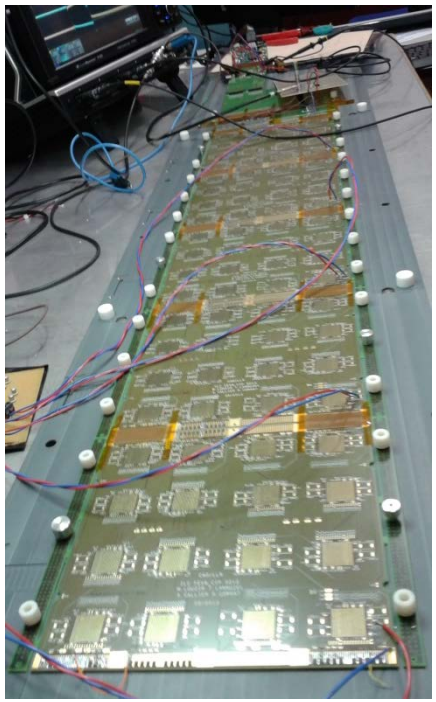
In principle, front-end boards will be chained forming up to 2m long detector SLAB, most of signals in bus

Issue 1 : clock distribution (5 & 50 MHz)
Interconnects are not impedance controlled (FFC)
One clock line may be loaded by 40 to 80 ASICS



large C-W structure exists

⇨ Use of MLVDS adapted with 100 Ω on both sides, 100 mVpp remaining signal at the end
(6 Ohms loss/board, 20-40 pF/board, up to 10 boards)
⇨ Next version ASIC will have a PLL generating the highest frequency



Issue 2 : Power distribution (12 A pulses) & blocking capacitors (tested with FET switches as loads)

⇨ Current taken from a 800mF super cap (16mΩ ESR) + 2mF/board

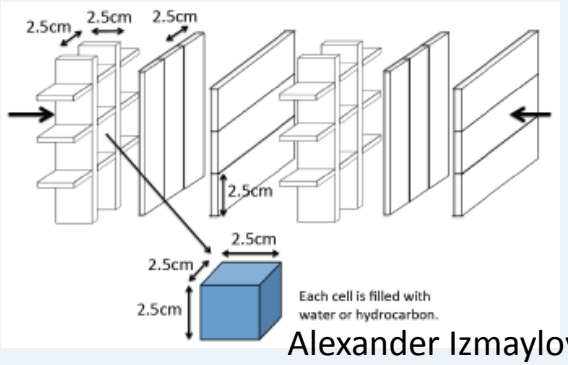
Along 6 boards, static loss is 250 mV due to connectors (w/o chips).
May forsee to distribute power in a star topology.

Would welcome any expertise in simulating current return paths and effects on chips.

Application to other projects

WAGASCI detector for T2K experiment

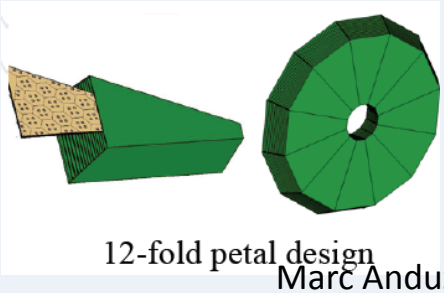
Scintillator + MPPC based detector, both water and plastic “absorber”.
Can keep same concept changing chip from SKIROC to SPIROC : same DAQ, similar FE. On going studies at LLR

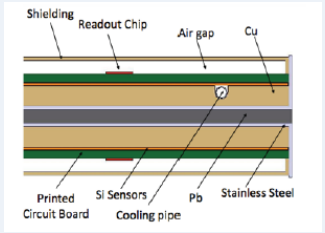


Alexander Izmaylov

Upgrade of the CMS ECAL end-caps

Completely different electronics but similar sensors (large PIN diodes matrix) & very similar mechanical structure build on carbon fiber composite (studied at LLR)

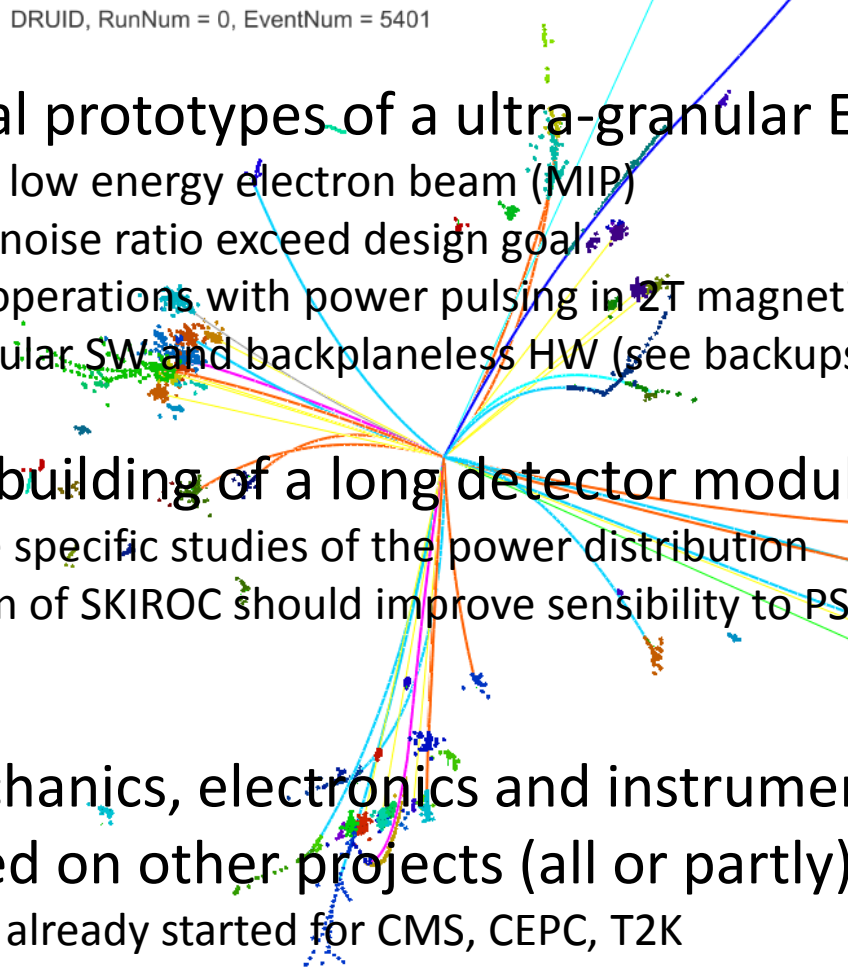




Marc Anduze, LLR

An ECAL for CEPC (Chinese e-e+ collider)
may also be based on the same concept, studies have started.

Conclusion



Technological prototypes of a ultra-granular ECAL designed for PFA

- Tested with low energy electron beam (MIP)
- Signal over noise ratio exceed design goal
- Successful operations with power pulsing in 2T magnetic field
- DAQ : modular SW and backplaneless HW (see backups)

Next step is building of a long detector module (10000 channels)

- Will require specific studies of the power distribution
- Next version of SKIROC should improve sensibility to PSRR and digital noise

R&D on mechanics, electronics and instrumentation can be reused on other projects (all or partly)

- Studies has already started for CMS, CEPC, T2K

References

CALICE collaboration NIM A 654 (2011), 97; e-print arXiv:1102.3454, R. Pöschl et al.

ILD ECAL group, V. Boudry et al, « Development of technological prototype of silicon-tungsten electromagnetic calorimeter for ILD », proceedings of TIPP'2014 to be published in NIM.

CALICE and EUDET Collaboration, C. de La Taille, "Performance of 2nd generation CALICE/EUDET ASICs," in Proceedings of 14th International Conference on Calorimetry in High Energy Physics (CALOR 2010), Beijing, China. 10-14 May 2010., vol. 293, p. 012016. 2011.

R. Pöschl, « Construction of a technological prototype for a highly granular electromagnetic calorimeter », Presentation au LCWS11 Grenade, Espagne, acte de la conférence et arXiv : 1203.0249 [physics.ins-det]

CALICE Collaboration, C. Adloff et al., "Tests of a particle flow algorithm with CALICE test beam data," JINST 6 (2011) P07005, arXiv:1105.3417 [physics.ins-det].

D. Jeans, J. Brient, and M. Reinhard, "GARLIC: GAmma Reconstruction at a LInear Collider experiment," JINST 7 (2012) P06003, arXiv:1203.0774 [physics.ins-det].

R. Cornat, Acquisition system and detector interface for power pulsed detectors, TIPP 2011 conference, t o be published in Physics Procedia, Elsevier.

R. Cornat «Technical R&D towards a Silicon-Tungsten EM calorimeter for ILD» talk given at Linear Collider Workshop 2013 (http://inspirehep.net/record/1262156/).

F. Gastaldi. A scalable gigabit data acquisition system for calorimeters for linear collider, TIPP 2014

Backups

Expectations for a DAQ system

- **Scalable**
  - Computing network architecture
- **Standard**
  - Giga-Ethernet
  - Serial 8b10B
  - Cables and connectors
    - Hdmi : 5 pairs + supplies
    - CAT5 or fibre
    - Backplane-less
  - Detector interface (DIF) unified among the detectors (CALICE standard)
- **Compact**
  - "one cable for everything" : Data Acquisition, Timing, Slow control
- Flexible (prototypes)
  - (re)programmable parts (fpga)
- Cheap : Off the Shelf components

R&D at LLR-Ecole Polytechnique / IN2P3-CNRS based on previous work from Univ. College London, Manchester Univ., Cambridge Univ., Royal Holloway

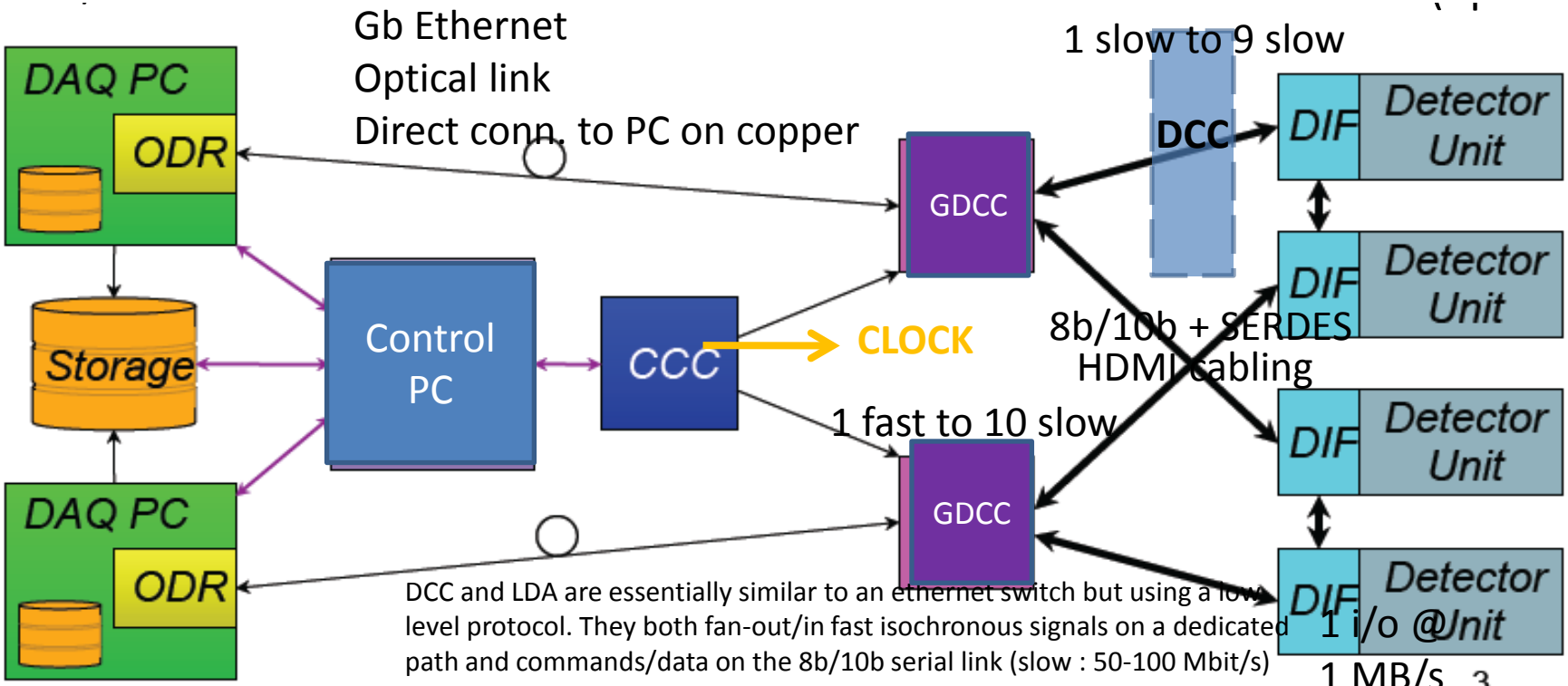
Limitations

- Low speed access to a chain of 10-100 very front end chips (1k-10k channels) : 1-5 Mbit/s
  - daisy chain and reduced number of connections for compactness,
  - up to 2 m PCB traces,
  - low power consumption at VFE chip level : open collector bus
- Therefore assume : auto trigger, zero suppression at VFE level
- TFC interleaved with SC, DAQ using 8b/10b protocol : limited timing precision (>10 ns)
- Events build at VFE level, read out during inter-spill train : limited buffering capacity (10-100 evt)

Low occupancy of the detectors is assumed (<0.5%/cell/bunch)

DAQ system overview

DIF : Detector InterFace (serial to parallel protocol)
DCC : Data Concentrator Card (fan out/in)
GDCC : Gb Ethernet DCC
CCC : Clock & Control Card (trigger, busy, fast commands)
ODR : Off detector Receiver (standard network card until now)
All links close to detector are based on 8b10b (16b20b) serial protocol (2 pairs, 50-100 MHz), escape K-characters used to transmit fast commands.



DCC and LDA are essentially similar to an ethernet switch but using a low level protocol. They both fan-out/in fast isochronous signals on a dedicated path and commands/data on the 8b/10b serial link (slow : 50-100 Mbit/s)

DAQ software (LLR)

Pyrame software suite designed at LLR (C++ core + Python) for DAQ and SC

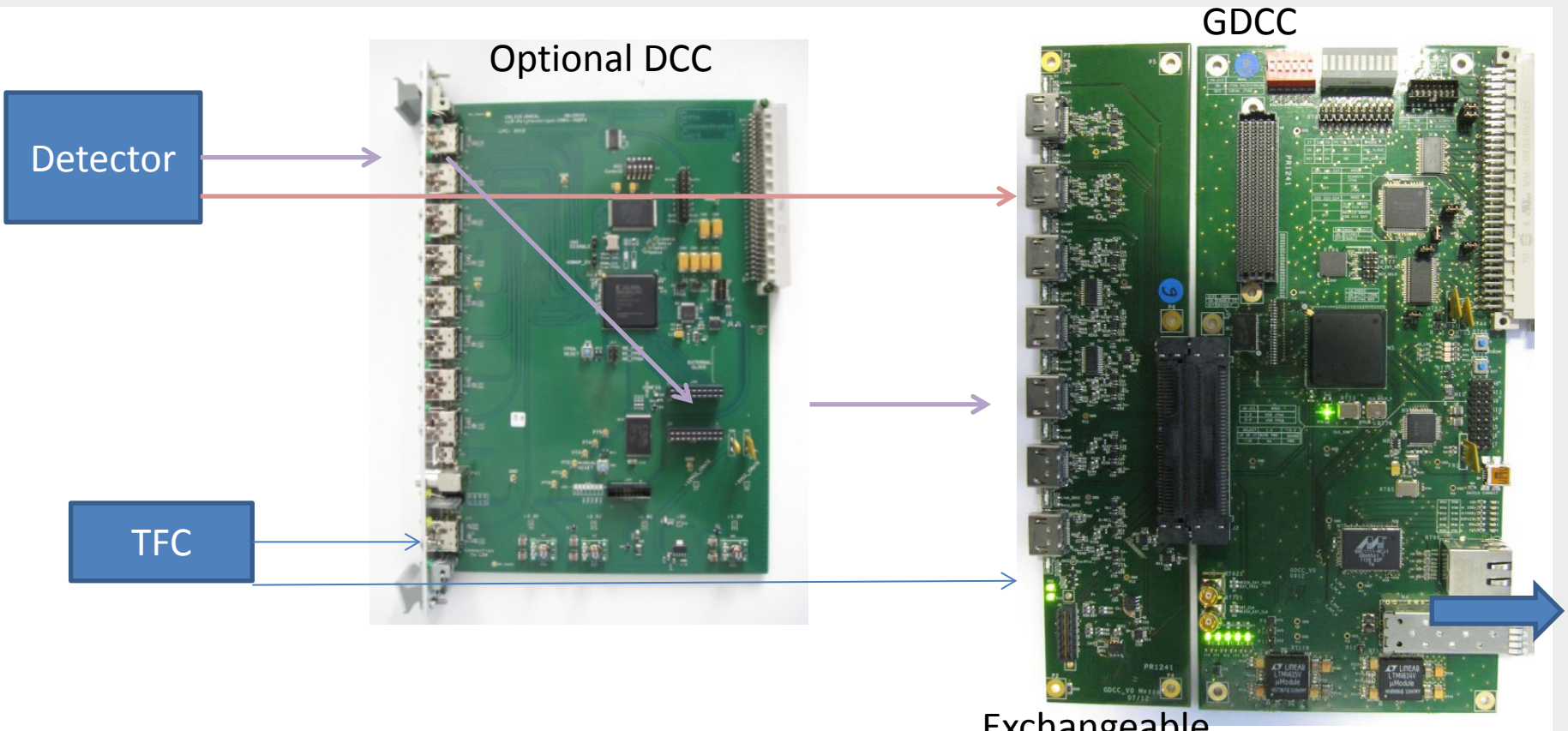
Acquisition chain with Multi-media distribution(files, sockets and shared memories)
Online event-building, Run Control and xml configurations
Used on GbEth networks

Slow control Highly modular and distributed : based on client-server architecture
Allows for remote control, multiple PCs
Control the detector electronics
but also the peripheral devices (power supplies, pulse gen., DCS…)
Provides a high level state machine for final user
Graphical interface
Scripting langage based on python

PYRAME will be open, currently shared within ECAL team
and CPPM (evaluation, in2p3 DAQ network)

“5% labview, 5% XDAQ, 5% PVSS, 85% simplicity…”

DAQ Hardware (LLR)



DCC has been used to distribute TFC for the 300 000 Channels of the CALICE SDHCAL

GDCC is in use on the CALICE Si-W ECAL

Low cost VME format (power only on J1)

Silicon-Tunsgten ECAL for ILD@ILC