Research and Design of the electronics system for the Underground Dark Matter Detection Experiment in IHEP

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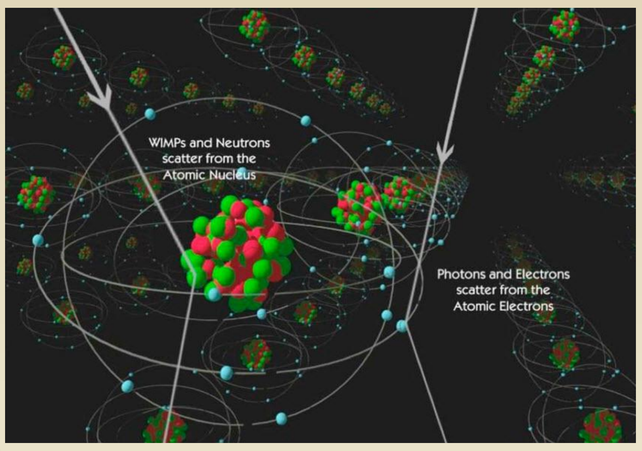
TWEPP 2014
22-26 September 2014
Aix en Provence, France

1·INTRODUCTION



The dark matter detection is an important issue in the field of the modern particle physics and astrophysics. The most possible component of dark matter is a new particle called weakly interacting massive particle(WIMP). The main mechanisms of WIMPs experimental detection are direct detection that detects the long-lived particle produced by the annihilation of WIMPs, and indirect detection that detects rare nuclear recoil event of WIMPs scattering on target material. The dark matter detection experiment in Institute of High Energy Physics (IHEP, Beijing) use indirect detection and choose CsI (Na) crystals as target material. Photomultiplier tubes collect the weak light and output analog electric signal.

According to the detector output waveform's characteristic (smallest amplitude:5mV, narrowest pulse width:20ns) and the requirement of distinguishing the single-photon from the Alpha signal, the construct of high-speed ADC module is determined. A 10bit, 1GSps ADC is chosen as the core sampling chip to meet the requirements.
High-speed ADC sampling will produce large amounts of raw data which needs to be transferred and real-time processed. The data acquisition system contains 2-level high-speed serial transmission and real-time processing based on Xilinx FPGA. The final data is transferred to the computer via the PCI-Express bus.

2·IMPLEMENTATION

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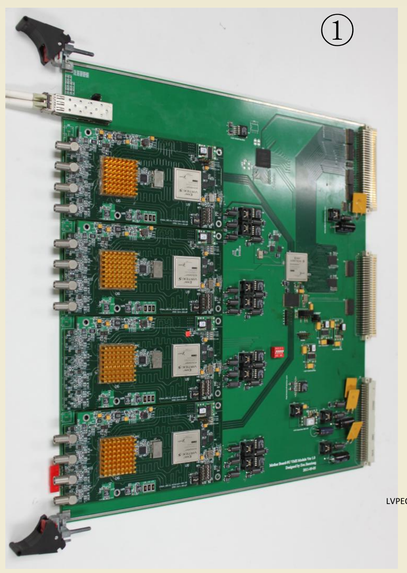

The high speed ADC module is a daughter-mother board structure. The daughter board is based on a 4-channel, 1Gsps, 10-bit ADC chip(EV10AQ190). A new automatic delay adjust method is used to capture the high speed data output of the ADC. A pipelined algorithm is used to realize the signal discrimination in the design. The over threshold signal is sent to the trig module. Besides, A self-test circuit is used to verify the ADC circuit working properly.
The mother board is a 9U-VME board. It collects data from 4 daughter boards and send it to the data acquisition system via a 1Gbps fiber with Xilinx Aurora 8B10B protocol.

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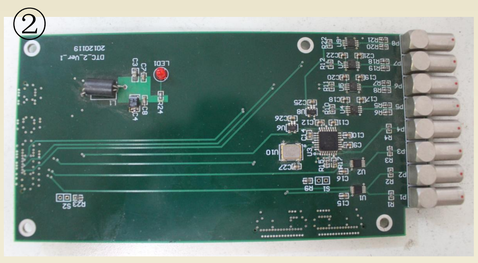
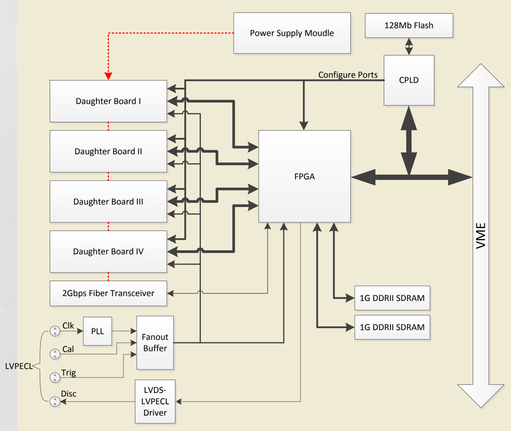
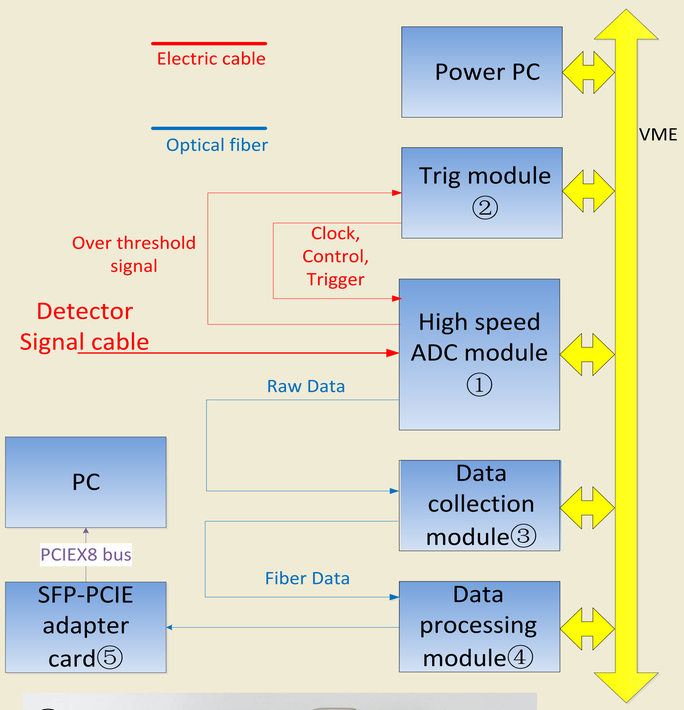


The trig module collects the over threshold signal from all the ADC modules in the whole crate and generates a global trigger, then fan out it back to all the ADC module.





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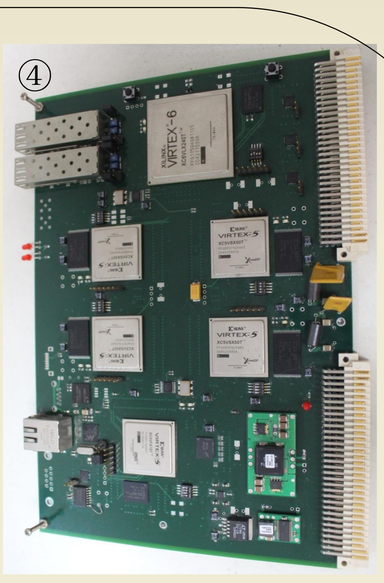

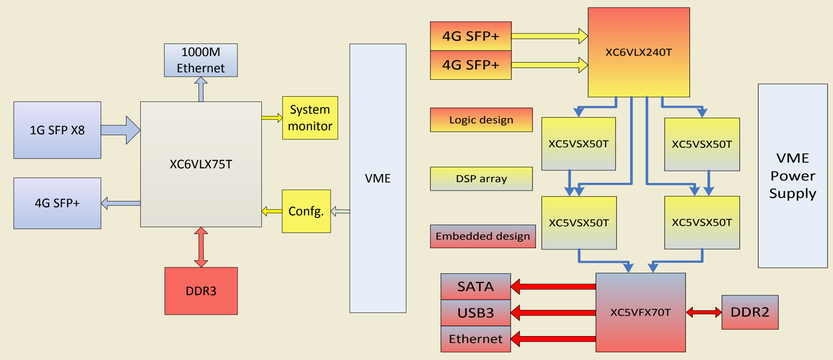

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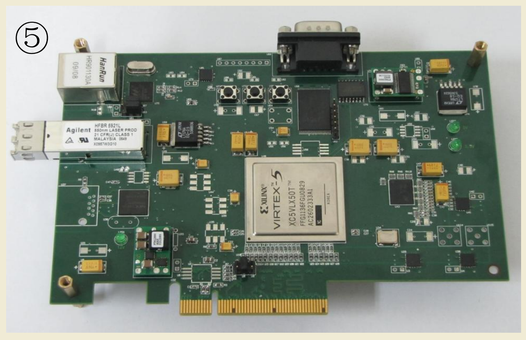
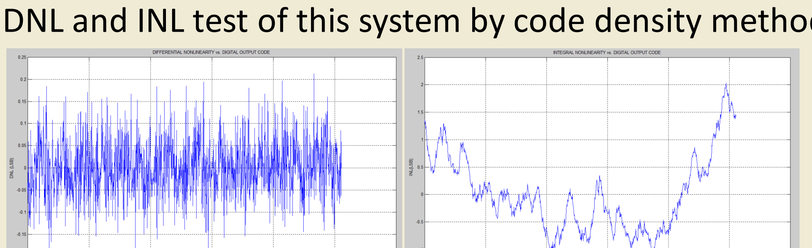


The SFP-PCIE adapter card is a PCIE X8 card. It receives the optical fiber data, then stored in DDR2. The final data is transferred to PC via PCI-Express bus.

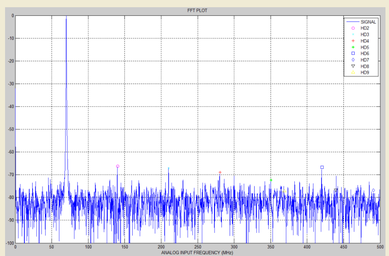
The backend digital data acquisition system has a 2-level data collection and processing structure. This structure uses two modules. The first one named data collection module collects the raw data from ADC module and processes the data Preliminarily, then transfers it to the second one. The second module named data processing module completes the complex algorithms including the compression, the integration and the real-time FFT. The data processing algorithms is achieved by the flexible DSP units in FPGA. A board-level cache by the memory chips is available to reduce the dead time of the system significantly.

3· PRELIMINARY RESULT

DNL and INL test of this system by code density method.

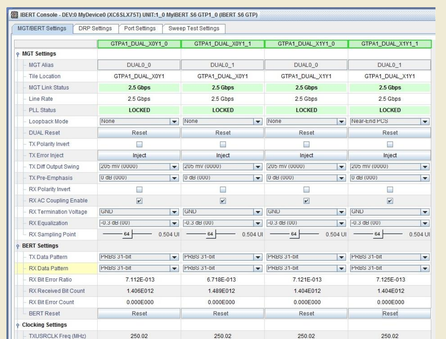


通道号	A	B	C	D
DNL(LSB)	0.22	0.27	0.25	0.23
INL(LSB)	2	1.5	2.1	1.75



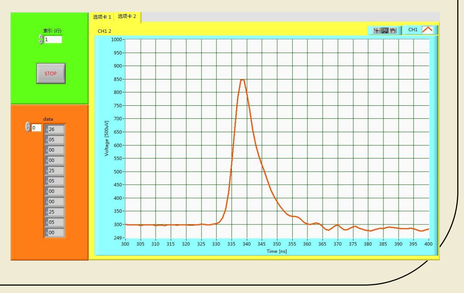
Dynamic performance test of the system using 70MHz, -1dBFS sine waveform input.

参数\通道号	A	B	C	D
THD(dBc)	-62.13	-59.61	-58.67	-64.78
SFDR(dB)	66.28	62.05	63.35	66.19
SNR(dB)	49.42	48.88	48.27	49.19
SINAD(dB)	49.19	48.57	47.90	49.07
ENOB	7.88	7.78	7.66	7.86



The working user interface by Labview.

Xilinx GTX BER test result
The BER of optical fiber link is less than 1.0E-12 with PRBS 31-bit test.



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