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Research and Design of the Electronics System for the Underground Dark Matter Detection Experiment in IHEP

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The underground dark matter experiment in IHEP is direct detection of dark matter that using CsI(Na) as detector material, and rare nuclear recoil events of dark matter particles scattering on target material will be detected by photo-multiplier tubes (PMTs). This paper describes the electronics system structure we chosen for this detector; emphatically focus on the design of main modules that are high-speed ADC module and 2-level data acquisition module. Some performance results also are presented at the end.

Summary

The underground dark matter experiment in IHEP is direct method of dark matter detection that using CsI(Na) as detector material, and rare nuclear recoil events of dark matter particles scattering on target material will be detected by photo-multiplier tubes (PMTs).

According to the detector output waveform characteristic and the requirement of high speed digitizing, the construct of high-speed ADC module is determined. The module is based in a 1Gsps, 10-bit ADC chip. A new automatic delay adjust method is used to capture the high speed data output of the ADC. A pipeline algorithm is used to realize the signal discrimination in the design.

Then we estimate the data acquisition bandwidth and the processing capabilities, and design 2-level data collection and processing modules based in Xilinx FPGA. The data acquisition system for the experiment can handle up to 40Gbps data bandwidth input and processing data.

Finally we measure the DNL and INL of ADC module by using the histogram method and the dynamic performance results by FFT analysis. Also we test the entire system performance with detector. The result meets the experiment requirement.

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