Dream: a 64-channel Front-end Chip with Analog Trigger Latency Buffer for the Micromegas Tracker of the CLAS12 Experiment

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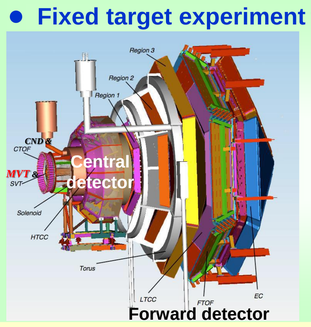
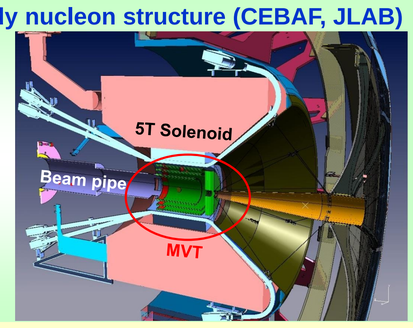
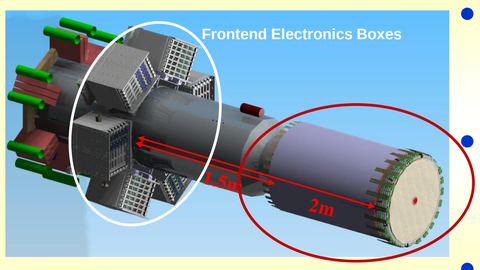
Architecture and Principles

Clas12 Micromegas Vertex Tracker

- Fixed target experiment to study nucleon structure (CEBAF, JLAB)



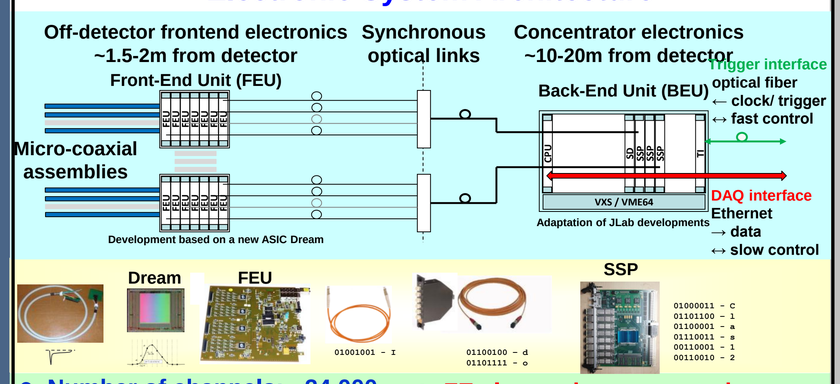




- Barrel: 6 cylindrical layers
  - →Coverage: 125°-35°, 2.7 m²
  - →Precision: O(100µ)
  - →~18 000 Z & C strips
- Forward: 6 disks
  - →Coverage 29°-6°, 1.3 m²
  - →Precision: ~100µ
  - →~6 000 X & Y strips
- Resistive Micromegas

Commissioning: partial in 2015, full in 2016

Electronic System Architecture

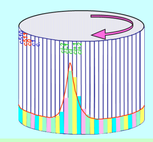


- Number of channels: ~24 000
- Physics background: 20 MHz
  - →Up to 60 kHz hit rate per strip
- Trigger rate: 20 kHz
  - →Trigger Latency: 16 µs
- Timing resolution: ~10 ns
  - → Charge measurements: 10-bit
- No room inside the magnet
- FE electronics connected to detector using low capacitance (43pF/m) microcoax cables (1.5m to 2m)
- Detector capacitances: 100-200pF
  - →Required Signal / Noise ~ 40
- off-detector area is still hostile
  - →Limited space, 1T field

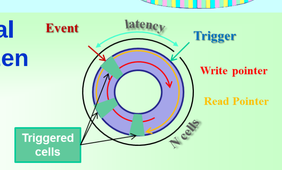
Challenging requirements with imposed off-detector frontend electronics

Principle of the FE: analog sampling in a deadtime free SCA

- similar to APV chip operation, but with extended capabilities
- 64 channels of 512-cell SCA each operated in //
- Signals are continuously pre-amplified, shaped, sampled and stored at 20-30 MHz in the circular analog memory

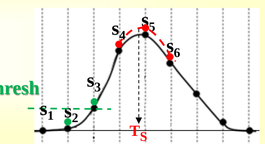


- For each event triggered (fix latency external trigger), n (programmable) samples are frozen
- Several events can be stored in the SCA
- SCA readout and digitization of selected samples of all channels @ 20 MHz



The 512-cell SCA is deep enough to compensate for a 16µs trigger latency & to store 45 4-sample events (20MHz read and write, 40kHz trigger) with a deadtime < 10^{-7}

- Selected samples are digitally processed
  - →Common noise subtraction (online by FPGA)
  - →Zero suppression (online by FPGA)
    - All samples of retained channels are readout
  - →Measure charge and time



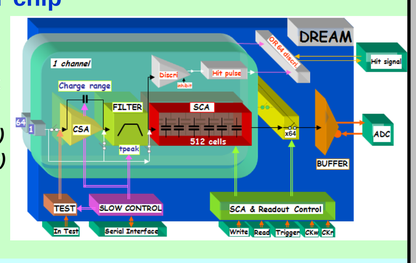
Pick-up (expected because of cables) immunity, precise time measurement

The Dream Frontend ASIC

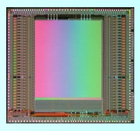
DREAM overview

Dead-timeless Read-out Electronics ASIC for Micromegas

- CMOS AMS 0.35µm technology (cheap, blocks reuse)
- Derived from the previous AGET chip
- 64 channels with each:
  - A CSA optimized for large C_{Det}
  - 4 gain ranges: 50fC, 100fC, 200fC, 600fC
  - 16 *peaking times: from 50 ns to 1 µs*
  - *512-cell SCA (1 to 40 MHz sampling rate)*
  - *Analog multiplexed output @20 (40 MHz)*
  - *Requires an external ADC*
  - *1 discriminator (common threshold)*
  - *Injection /test system*



- LVDS self-trigger output available (not required for CLAS12)
  - *Comparison of the multiplicity signal (number of triggered channels) with a programmable threshold (from 1 to 55 channels)*
- SPI link for configuration
- On-chip SCA controller
- 128-pin 0.4 mm package easy to handle
- Inputs located by groups of 32 on 2 opposite sides

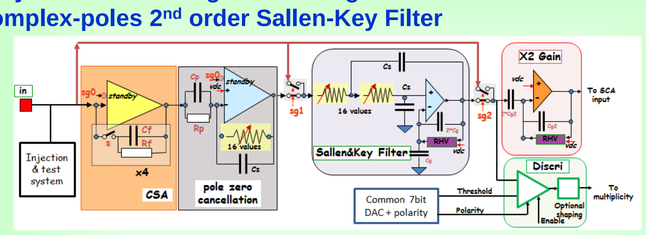


AMS 0.35µm, 65 mm²
700.000 transistors

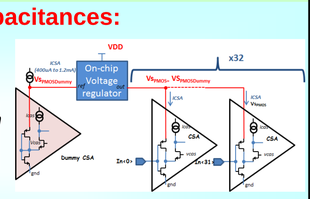
A versatile chip suited for different detector types with dead-time free operation

Very Front End Part

- Very Standard analog chain using Pole zero cancellation and complex-poles 2nd order Sallen-Key Filter



- *Main parameters programmable*
- *CSA or (CSA + filter) can be bypassed, CSA can be disabled channel/channel*
- *2 possible CSA decay constants:5 (high rate) and 50µs (lower noise)*
- Innovative CSA design for High Input Capacitances:
  - *>80dB OpenLoop gain required for charge transfer*
  - *Folded cascode configuration*
  - *new: input transistor replaced by an Inverter:*
    - *→ Usually Input transistors are in weak-moderate inversion => No benefit to increase the input transistor size*
    - *→ Here both P&N transistors contributes to the input gm*
    - *→ Serie Noise improvement by 30% / single transistor*
    - *→ Same improvement than ~ doubling the current in the input branch*
  - *Inverter bias (400µA to 1.2mA) ensured by a 2 on-chip low noise voltage regulator common to 32 channels providing a source voltage for the PMOS generated by a dummy CSA*



A versatile and innovative very front-end

Deadtime-free operation of the analog memory

On-chip scalable logic driven by 5 signals:
- * Init: initializing all the sequencers
- * WCk: sampling clock,
- * Trig: synchronous fix-latency trigger
- * Read: Event Read request,
- * Rck: sequences the read operation (incl channel multiplexing,)

Mainly Organized in 512 columns each generating the write & read commands common to all the channels for the cells corresponding to each time bucket ,

Two 9-bit Gray code counters used for write and read event numbers (driven by Trig & Read),

Column write commands generated by shift register (SR) with a single bit circulating and clocked by WCk ,

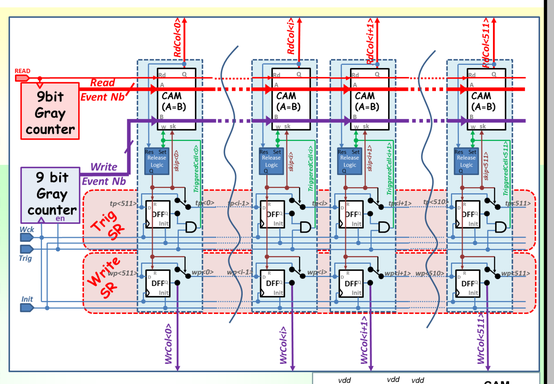
Similar SR(shifted to compensate for trigger latency) used to freeze the triggered cells. The frozen columns of the two SR are skipped ,

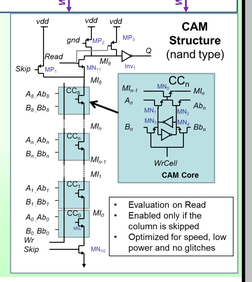
On Trigger, Write event number stored in the Content Addressed Memory (CAM) of the column frozen by the trigger ,

On Read rising edge, the column with the CAM storing a data equal to the Read Event number is read and then released after the end of its readout,

Write event number and physical column index sent in the data flow + error detection if no event found @ Read request ,

No limitation of number of samples / event : each sample is treated as an event





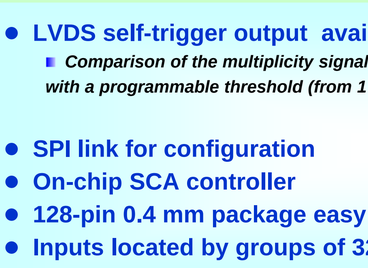
CAM-based skip logic

Performances

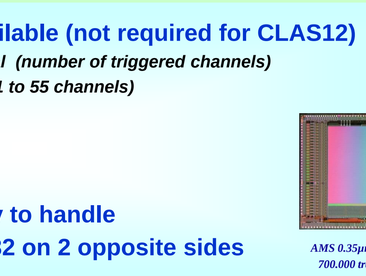
Test Bench Measurements (prototype of the FEU board)

DREAM behaves as expected :

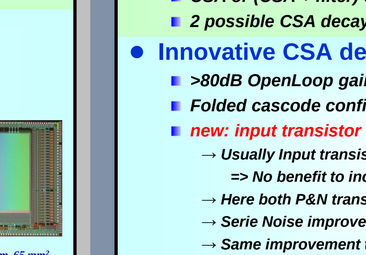
- *Several hours of operation in the CLAS12 conditions (20 kHz trigger rate, randomly distributed, 4 samples/event 20MHz write and read clock) without any deadtime or error,*
- *Self –triggering capabilities demonstrated,*
- *All analog parameters matching simulation results in all the various modes of the chip*
- *10mW/channel power consumption (3.3V power supply)*



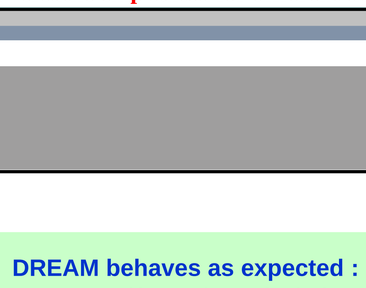
Dream response to a ~70fC charge for various programmed peaking time (200fC range) : the variation of amplitude is expected from the design



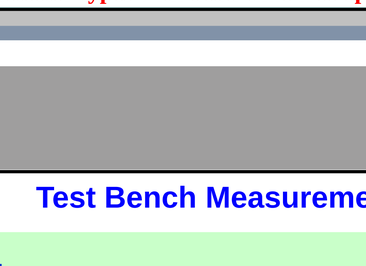
Very small variation of the gain as a function of the input capacitance:
Open-Loop Gain > 20 00 (200fC range)



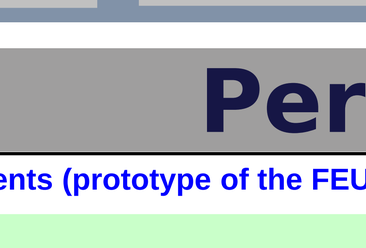
Gain uniformity within a chip is better than 0.6% RMS



Transfer function for few channels of a chip (200fC mode, tp= 180ns). The baseline was set to ~500 ADU. The saturation is due to ADC



Linearity (200fC): extracted from linear fit of the previous plot. Better than 1% on the full range.
Error bars are related to the injection DAC precision



ENC vs CDET simplified linear parametrizations for the 200fC range, 5µs CSA decay time

Equivalent Noise Charge vs Filter Peaking Time for various detector capacitances in the 100fC mode and 5µs decay time of the CSA.

As targeted, the ENC is lower than 2500 e- RMS for tp< 200ns and CDET< 230pF and fulfill the CLAS12 requirements

The symbols are for measurements and the line are results of a fit based on the standard parametrization of front-ends:

$$ENC^2 = \frac{\alpha^2 (I_{POLes}) \cdot (C_0 + C_{in})^2}{t_p} + \gamma^2 \cdot (C_0 + C_{in})^2 + \beta^2 t_p + ENC^2_{2ndstage}(Range)$$

Parameter Name	Value	Unit	Comment
α(1.2mA)	120	e-.ns$^{1/2}$.pF^{-1}	Serie noise coefficient
β (100fC range)	25 ($\tau_{decay\ CSA}$ =5µs) 6 ($\tau_{decay\ CSA}$ = 50µs) Scales as Range$^{1/2}$	e-.ns$^{1/2}$.pF^{-1}	// noise coefficient
γ	2	e-.pF^{-1}	1/f noise coefficient
C_0	30pF	pF	
$ENC_{2nd\ stage}$	390 (100fC range) Scales as Range	e-	2nd stage noise

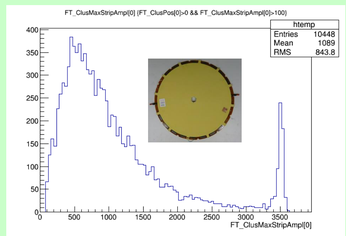
All the values are consistent with our expectations, excepted a 25% excess for serie noise
But the measured serie noise corresponds to only:
- **a noise voltage density of only e_n= 0.7 nV/Hz$^{1/2}$**
- **Or an equivalent noise resistor of 30 Ohm**

This noise is only 10% higher than those of an ideal BJT biased with the same current.

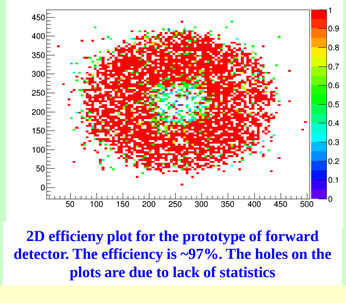
This validates our new CSA design

Measurements with detectors

CLAS12 forward Detector under test inside the Saclay cosmic ray telescope. Note the 2m cables connecting the detector to the FE electronics crate



MIP charge spectrum measured on the forward detector with DREAM in this setup. The signal is clearly out of the noise (<2500 e- = 8 ADU RMS)



2D efficieny plot for the prototype of forward detector. The efficiency is ~97%. The holes on the plots are due to lack of statistics

Conclusion & Perspective

- *The DREAM ASIC has been manufactured, tested and validated for its use in Micromegas tracker of CLAS12,*
- *A production batch has been delivered in sept 2014 for CLAS12,*
- *Its versality , the unprecedented depth of its buffer and its new features make it a good alternative to the APV chip, especially for detectors with large capacitances*
- *It is already used or planned for several other experiments/setup using Micromegas detectors (ASACUSA, GBAR, muon tomography)*

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