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Dream: a 64-channel Front-end Chip with Analogue Trigger Latency Buffer for the Micromégas Tracker of the CLAS12 Experiment.

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The new 64-channel DREAM (Dead-timeless Readout Electronics ASIC for Micromégas) chip has been designed to read the Micromégas tracker of the CLAS12 experiment. Each channel associates a low noise very frontend part, optimized for large detector capacitances (150pF range), together with a 512-cell analogue memory, ensuring both a trigger latency and derandomization bufferization, allowing a negligible deadtime in operation, in the conditions foreseen for the experiment (20 MHz sampling and readout frequencies, 20 kHz trigger rate, and up to 16µs trigger latency). The paper describes the chip architecture and reports its main measured performances.

Summary

In the frame of the upgrade of the Jefferson Lab (Virginia, USA) electron accelerator to 12GeV, the existing Cebaf Large Acceptance Spectrometer (CLAS) of Hall B prepares a major upgrade to reach $10^{35} cm^{-2}.s^{-1}$ luminosity, leading to the construction of a new Central Tracker using approximately $4m^2$ of Micromégas detectors for its outer barrel and forward parts. The Micromégas barrel consists of three double layers of stripped cylindrical Micromégas, each made of three curved tiles with active area up to $50 \times 45 cm^2$. The Micromégas forward tracker is a set of 6 disk-shaped Micromégas with 43cm radius. The two trackers will be located inside the intense 5T magnetic field of a solenoid, while for an easier design and maintenance, the corresponding 25.000 frontend electronics channels, will be installed in racks, 1.5m away, via ultrathin coaxial cables.

The total capacitance at the front-end electronics input thus yields up to 180pF. Because of the expected background rate of 50kHz/strip and trigger rates of 20kHz, the noise and shaping performances required for the very frontend electronics to reach a good tracking efficiency are quite similar to those of the SFE16 chip used for the Micromégas tracker of COMPASS, but for an input capacitance two times higher, and a large pickup noise induced by the large detector size and the cable length. Instead of the SFE16 binary chain, an analogue readout was chosen, allowing common mode subtraction and centroid calculation after digitization. As no available chip fulfilled these requirements, we designed a new chip, named DREAM, using the AMS 0.35µm CMOS technology. This chip integrates 64 channels, each consisting of a charge sensitive preamplifier - using a new structure optimized for large detector capacitances - a shaper, which output is sampled in a 512-cell circular buffer Switched Capacitors Array and also connected to a discriminator. For every channel, the samples marked by the fixed latency trigger are readout asynchronously, serialized and digitized by an external 20MHz 12-bit ADC without stopping the sampling process. This operation is managed by an on-chip controller based on Content Access Memories and permits to keep the deadtime due to DREAM lower than 10^{-7} for a 4 samples/event readout, a 40kHz trigger rate and a 16µs trigger latency. The common mode noise subtraction and zero suppression operation are performed off-chip. The DREAM chip has been designed to be versatile and reusable with other detectors or in other experiments, thanks to a SPI link to set its main parameters (shaping time between 70ns and 1µs, dynamic range between 50fC and 600fC, sampling frequency between 1 and 40MHz, number of samples/event). An LVDS output providing the or of the discriminator outputs is also available for trigger generation. The final paper will detail the chip architecture and report the performances measured on prototypes of the front-end and acquisition electronics and detectors.

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