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Zero Suppression Logic of the ALICE Muon Forward Tracker Pixel Chip Prototype PIXAM and Readout Electronics Development

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In the framework of the ALICE experiment upgrade at HL-LHC, a new tracking detector, the Muon Forward Tracker, is foreseen. To fulfill detector requirements, CMOS Monolithic Active Pixel Sensor (MAPS) technology was chosen thanks to interesting performances and properties in terms of readout speed, spatial resolution, radiation hardness, granularity, power consumption and material budget. This paper presents the large size prototype PIXAM, designed in a 0.18 µm process, and will focus specially on the zero suppression logic of the chip which does the data compression. Finally, the readout electronics principle of the compressed data flow is also presented.

Summary

In the framework of the ALICE experiment upgrade at HL-LHC, a new forward tracking detector, the Muon Forward Tracker (MFT), is foreseen to overcome the intrinsic limitations of the present Muon Spectrometer and will perform new measurements of general interest for the whole ALICE physics.
To fulfill the new detector requirements, CMOS Monolithic Active Pixel Sensors (MAPS) provide an attractive trade-off between readout speed, spatial resolution, radiation hardness, granularity, power consumption, and material budget. This technology has been chosen to equip the Muon Forward Tracker and also the vertex detector: the Inner Tracking System (ITS). Since few years, an intensive R&D program has been performed on the design of MAPS with the 0.18 µm CMOS Image Sensor (CIS) process. In order to avoid pile up effects in the experiment, the classical rolling shutter readout system of MAPS has been improved to overcome the readout speed limitation. A zero suppression algorithm, based on a 3 by 3 cluster finding (position and data), has been chosen for the MFT. This algorithm allows adequate data compression for the sensor. This paper presents the large size prototype PIXAM, which represents 1/3 of the final chip, and will focus specially on the zero suppression block architecture with simulation results. This chip is already designed and under fabrication in the 0.18 µm CIS process. Finally, the readout electronics principle to send out the compressed data flow is also presented taking into account the cluster occupancy per MFT plane for a single central Pb–Pb collision.

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