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Progress Towards the First Prototype of a Silicon Tracker Using an 'Artificial Retina' for Fast Track Finding

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Our research aims to develop a specialized track processor capable of precisely reconstructing events with hundreds of charged-particle tracks in pixel and silicon strip detectors at 40 MHz. For this purpose we design and test a massively parallel, neurobiology-inspired, pattern-recognition algorithm. Here we present the R&D for a first prototype of silicon tracker with trigger capabilities based on this novel approach for fast track finding. We report on the design and the construction of a practical device that consists of a telescope based on silicon strip detectors. The track finding algorithm has been implemented using commercial FPGA of TEL62 boards. Tracking performance and trigger capabilities of the device are presented along with perspective for future applications.

Summary

The "artificial retina" processor is an FPGA-based device for the online reconstruction of charged-particle tracks in pixel and silicon strip detectors in high multiplicity events at 40 MHz. The working principle is inspired by the mechanism that, according to current understanding, underlies the early stages of visual-information processing in the primary visual cortex of mammals, and is based on the extensive parallelization of data distribution and pattern recognition algorithm. The progress towards the design and the construction of the first prototype of silicon tracker using the artificial retina algorithm for fast track finding is presented here. It has been implemented in commercial FPGAs in three main logic modules: a switch for the detector hits, a pool of engines for the digital processing of the hits, and a block for the calculation of the track parameters. The switch module distributes in parallel the hits from all the detector layers to appropriate logical units, called engines, which determine the good match ('weight') of the hits combination with a specific track hypothesis. The engine corresponds to a specific receptor of the grid of the track parameter space ('retina') and its excitation is proportional to the weight calculated by the engines. Each engine interacts with the neighbouring engines to determine the maximal weight value and then another logical block interpolates the track parameters from other two adjacent engines in the appropriate direction.

The telescope consists of 8 layers of single-sided silicon strip detectors with 512 strips each. The detectors can be placed alternately with the strips in vertical and horizontal directions in order to reconstruct the x and y coordinates or with strips in one direction in order to have 8 measurements in a single coordinate. The detector size is about 10 cm x 10 cm and the strip pitch is 183 um. The detectors are read out by the Beetle chip, a custom ASICs developed for LHCb, which provides the measurement of the hit position and pulse height of 128 channels.

The read-out boards are based on FPGAs Xilinx Kintex 7 lx160, each one connected to 4 ADCs with 8 serial outputs at 80 MSPS. They manage the read-out ASICs and the sampling of the analog channels. The read-out is performed at 40 MHz on 4 channels for each ASIC that corresponds to a decoding of the telescope information at 1.1 MHz. Moreover, the FPGA accomplishes the suppression of zero data and implements a part of the switch. For the processing stage a TEL62 board has been used. This processor is equipped with 4 Altera Stratix III FPGAs that provide adequate computing performance to implement the rest of the switch, the engines, and the interpolation for determining the track parameters. The parameters of the tracks detected are

finally transferred to host PC via Ethernet lane at 4 Gbit/s over UDP. The tracking performance of this device has been simulated and found to be comparable to offline results but with sub-microsecond latency.
The system is modular and can be designed for high energy physics experiments with large tracking volumes and high rates. According to simulation studies the artificial retina processor is capable reconstruct tracks in real time in high multiplicity events at 40 MHz with offline-like track quality.

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