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Development of the Readout System for LCTPC for the Future ILC

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We will present the readout system being designed for the LCTPC (Large Prototype TPC) for the future ILC. A CPLD resident on a MCM(Multi-chip Module) board will be used to concentrate data from 8 SALTRO chips on the same board and transfer them to a SRU(Scalable Readout Unit) via a serial DTC(data, trigger, control) link, in the final system there will be 75 MCM boards sit on 3 pad module make 9600 analog channels in total. We will report the status of the first MCM prototype board as well as the full readout chain.

Summary

In this contribution, we will report ongoing development and test results of the readout system designed for the LCTPC (Large Prototype TPC) based on the MPGD (Micro Pattern Gas Detector) technology for the future ILC (International Linear Collider). The feasibility of the MPGD, with respect to the requirements set by the physics challenges at the future ILC has been demonstrated in the EUDET project. We are now in the phase (AIDA) of developing a readout system which should essentially meet various requirements of the final readout electronics.

The present number of SALTRO-chips only allow to equip 3 pad modules, out of 7, in the large prototype TPC. The chips are mounted on MCM-boards, with 8 chips on each board. The MCM-boards are arranged in a 5x5 matrix on each pad module i.e. in total there will be 25 MCM-board on a pad module. Each SALTRO-chip, developed at CERN, can shape, digitize and process 16 analogue signals from the detector with a 10-bit dynamic range and the sampling rate can be selected in the range 5 - 40MHz. The 128 analog channels data, from eight SALTRO-chips on an MCM-board, will be concentrated by a CPLD and transferred to the SRU(Scalable Readout Unit) through one DTC(Data-Timing-Control) link. Slow control communication with DCS and data readout to common DAQ system are implemented by two separated Gbe link on the SRU, a single SRU can handle up to 40 MCM boards in maximum. The SRU interfaces with TLU(Trigger Logic Unit) which provides common triggers and timing information as well.

The silicon die of the SALTRO chip is 8.7x6.2 mm² and contains 16 readout channels which equals an occupancy of 3.37 mm² per channel.

It is unrealistic to assemble untested dies directly on a pad module and expect that all chips will work. The alternative of using packaged chips is not a realistic choice since it requires too much space on the pad board. In order to give small enough pad sizes, the dies will be mounted on Carrier Boards, only slightly bigger than the chips themselves, which simplifies the handling and allows individual chips to be tested. The size of the Carrier Boards is 12.0x8.9 mm², eight of these carrier boards are mounted on one MCM in a size of 32.5x25 mm² using BGA soldering techniques.

The MCM-board is a very dense board and not ideal for testing and debugging. We have therefore produced a MCM prototype board with only one packaged SALTRO installed on, in a size of 210 x 145 mm² which is suitable for lab works, to initiate the CPLD firmware design and the implementation of the full readout and control chain.

We will report the full DAQ chain set-up and the performance of the first MCM prototype board as well as the first test result of the SALTRO chip.

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