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Readout Electronics Upgrade on ALICE/PHOS Detector for Run 2 of LHC

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The ALICE PHOS collaboration is carrying out a major upgrade of its readout electronics for the RUN 2 of LHC (2015-2017). The upgrade mainly includes three aspects: 1) The increase of the event readout rate; 2) The improvement of the communication stability of the interface between Front-end electronic boards and readout concentrators; 3)The compatibility to the upgraded ALICE Trigger system and DATE software. We will present the latest status of the upgrade activities, with particular focus on the technical implementation strategies and the test results.

Summary

Coming towards Run 2, PHOS is considering a higher event readout rate. The PHOS readout electronics used during Run 1 of LHC (2009-2013) consisted of 28 Front-End electronics (FEE) boards and one readout concentrator (Readout Control Unit, RCU) per readout partition. RCU has two parallel readout branches, each branch has 14 FEE boards. 896 signal channels on 14 FEE boards are read out sequentially by the RCU through a single readout bus on the GTL backplane. The highest event readout rate (all the events are empty) is limited to about 3 000 events per second. In order to overcome the data throughput limitation, the RCU is now replaced by the Scalable Readout Unit (SRU), whose hardware is developed within RD51 project. Each FEE board now interfaces with SRU through a custom DTC (Data-Timing-Control) link over a shield CAT6 cable at a bandwidth of 160 Mbps. The SRU FPGA firmware has been specially designed to be compatible with the PHOS readout configuration and ALICE online system. The FEE FPGA firmware has been upgraded to support DTC interface. And a light real-time data suppression algorithm (Low gain channel suppression algorithm) has been designed and implemented in the FEE FPGA firmware which doubles the PHOS event readout rate. With latest SRU and FEE FPGA firmware, 30 kHz event readout rate for empty events has been achieved in PHOS lab at CERN.

The upgraded PHOS readout electronics also increases the stability of the communication interface between FEE card and readout concentrators. In the old PHOS readout electronics where many FEE boards share one common GTL backplane, a single bad FEE card sometimes affects the communication between RCU and other FEE cards on the same GTL backplane. In the new PHOS readout electronics, the GTL backplane is removed and each FEE board interconnects with SRU through an independent shield CAT6 cable. Therefore, the faults caused by the local bus failure are eliminated. In addition, this widely used commercial cable also greatly reduces the difficulties of the electronics maintenance in future.

The ALICE Technical Coordination has decided to go ahead with the RoE (Run over Error) strategy, which is heavily based on the fast EOR/SOR procedure. This new feature will allow the ALICE operator to start a new global run with a potentially very short delay by not resetting and restarting the Detectors. Accordingly, the ALICE Trigger system and DATE software are upgraded. The number of trigger classes sent to detectors is extended from 50 to 100. The format of DAQ Common Data Header (CDH) of the detectors to be provided is changed. In order to be compatible with the new Trigger system and DAQ system, the handling of ALICE trigger data and CDH has been upgraded in the SRU firmware, and it is being tested when the Trigger system and DATE software are upgraded next month.

We will present the latest status of the new PHOS readout electronics, with particular focus on the technical implementation strategy and test results.

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