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Development of a Five Channel, 12 bit, 800 MSPS µTCA-Based Digitizer For the Muon g-2 Experiment at Fermilab

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We present the design of a 5 channel 800 MSPS uTCA based digitizer that will be deployed in the the Muon g-2 Experiment at Fermilab. The digitizer features 12-bit 800 MSPS digitizers with dedicated 1Gbit memory buffers. Multiple Xilinx Kintex-7 FPGAs provide the control and coordination within the digitizer. Provisions for a modular front end allow for application specific analog signal conditioning prior to digitization. The design conforms to the AMC standard for a full size, dual module. We will also discuss initial test results.

Summary

A new waveform digitizer has been designed to support the efforts of the Muon g-2 Experiment at Fermilab. This digitizer features 5 independent channels of 800 MSPS, 12 bit digitization with dedicated 1 Gbit DDR3 SDRAM memory buffers. The design takes the form of a full size, dual height AMC card, which is installed into a µTCA crate. Each digitizer is a modular system that allows for custom front end signal processing. Control and coordination within the digitizer is accomplished using multiple Xilinx Kintex-7 FPGAs. This approach allows application-specific readout, storage and control. The board readout occurs via a 5 Gb serial links across Fabric B of the uTCA backplane. For deployment in the Muon g-2 experiment, an AMC13 module controls the readout and receives the data. The AMC13 was designed for CMS experiment at CERN, and is installed in the second, redundant, MCH slot, The digitizer can be triggered via front panel connections or across the communication links within the µTCA crate. The sampling clock is derived from copper or optical clock inputs on the AMC13 module or from a local front panel connection. Diagnostics and control interfaces are available via the TTC link to the AMC13, µTCA Gigabit Ethernet link to the MCH, or the RS-232 connection on the front panel.

We have designed and built a single channel prototype of the design at Cornell. This prototype has demonstrated basic data transfer and system controls. It is being used to develop the firmware to support the 5 channel design. The 5 channel version is designed and prototypes are presently being fabricated. These prototypes will be used in support of an end-end calorimeter test beam run at SLAC in July.

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