The eCDR-PLL IC, a Radiation-Tolerant ASIC for Clock and Data Recovery and Deterministic Phase Clock Synthesis

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Introduction – eCDR-PLL ASIC in the LHC environment

The LHC clock and trigger distribution systems (TTC), require recovering the timing signals with fixed and deterministic phase and low-jitter. Very few Components-Off-The-Shelf (COTS) can provide such functionality but none of them are radiation tolerant, forcing users to build workaround solutions when designing new systems. The eCDR-PLL ASIC is based on the eCDR IP block (F. Tavernier, 2013) and is being implemented to fulfil this need, featuring:

- Radiation tolerant design with deterministic phase and low jitter (< 10 ps rms)
- Two Frequency Multiplier (FM) modes by selecting the clock division ratio
  - 40, 60, 120 and 240 MHz output clocks with 260 ps phase-shift resolution (VCO @ 240 MHz), targeting the 4.8 Gb/s GBT-like link applications
  - 40, 80, 160 and 320 MHz output clocks with 195 ps phase-shift resolution (VCO @ 320 MHz), targeting typical TTC and e-link applications
- Clock and Data Recovery (CDR) mode with two initial calibration modes
  - Internal VCO calibration by means of a switched capacitor Wien-bridge, requiring no external clock input
  - External calibration, using a 40, 80, 160 or 320 MHz clock input
  - 40, 80, 160 or 320 Mb/s data rates operation modes with generation of 40, 80, 160 and 320 MHz clock outputs, independently of the calibration mode
  - Fine data and clock deskew with 195 ps resolution
- Typical applications
  - Fixed and deterministic latency based systems, regardless of the environment
  - Clock synthesis for Back-End (e.g. GBT-FPGA) and Front-End (e.g. GBTX e-link) applications, by selecting the FM mode
  - CDR for TTC decoders and jitter cleaner in radiation environment (e.g. IGLOO2 FPGAs)
  - Dual data-rate applications

Key Features

- Clock synthesis and CDR for Back-end and Front-end applications
- Fully radiation-hardened
- < 10 ps rms jitter
- SLVS and LVDS compliant inputs
- SLVS outputs compliant with FPGAs ref. clock inputs
- Programmable output driving current
- I^2C interface
- 1.2V supply voltage
- -20ºC to 100ºC temperature range
- QFN 5x5mm-32 L package

Phase Detector + Frequency Detector

Used in CDR mode, an Alexander Phase Detector (PD) determines whether the VCO clock is early or late (bang-bang decision). A rotational Frequency Detector (FD) is added to increase the data acquisition range up to ±25% of the data rate.

Control Block

The Control Block holds the power-up state machines and watch-dogs, automatically controlling the CDR/PLL core. Depending on the selected mode, the correct control signals are applied, disabling unused modules in order to save power.

Switched Capacitor Wien-Bridge

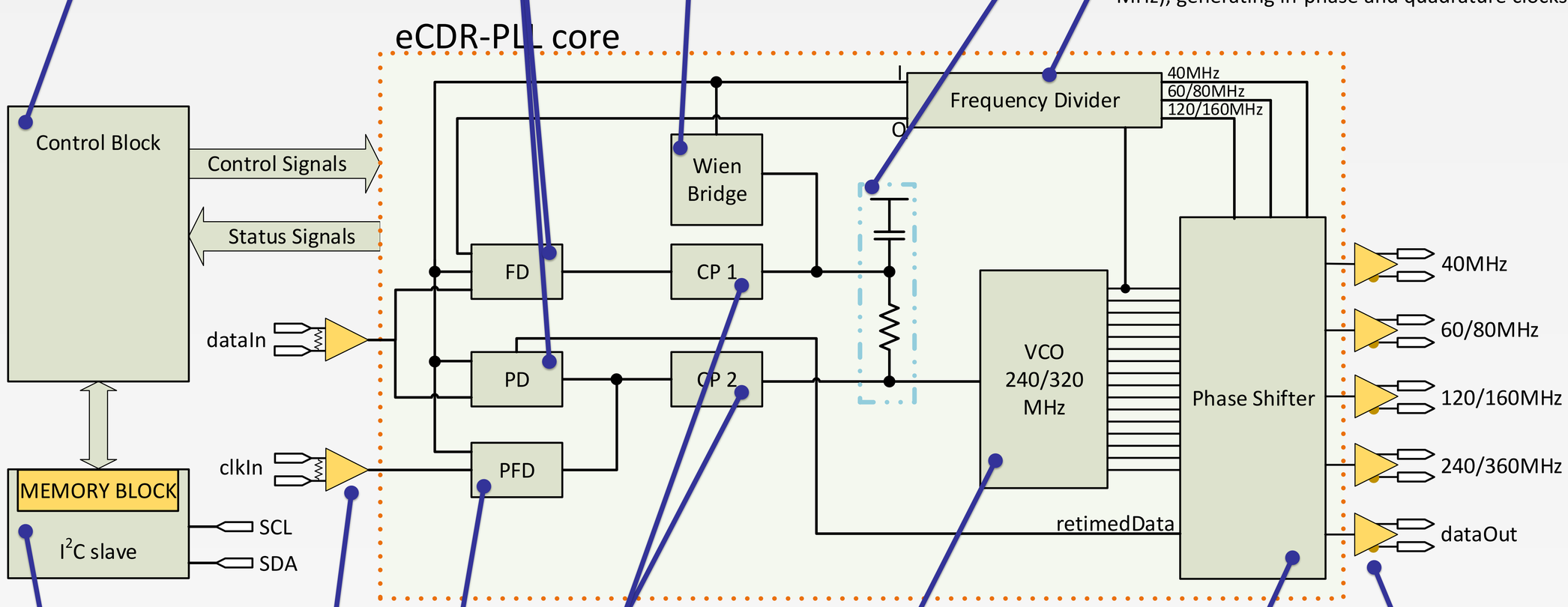
Only active during CDR internal calibration. It can be fine-tuned by means of programmable trim-resistor and achieves less than 100 ppm/ºC variation of the VCO frequency from the pre-set frequency.

1st order loop filter

Programmable RC time constant to optimize the loop dynamics.

Frequency Divider

Programmable frequency divider with different clock rates (40/80/160/320 MHz or 40/60/120/240 MHz), generating in-phase and quadrature clocks.



Charge pumps

Charge pumps with 3-bit programmable output current drive the 1st order loop filter.

VCO

8-stage differential voltage-controlled ring oscillator, generates 16 equally spaced clock phases. Unused phases can be disabled to reduce power consumption.

E-link outputs

The e-link output buffers are SLVS compliant with programmable driving current and compatible with FPGAs reference clock input. The data is pushed-out in the falling edge of the clock, providing optimal sampling point in the receiver.

Communication

The 7-bit I^2C slave module allows full control over the ASIC.

Phase and Frequency Detector

The PFD has an nearly unlimited acquisition range. It is in use in FM mode and during CDR external calibration.

E-link inputs

The data and clock e-link inputs are SLVS and LVDS compliant with a programmable on/off on-chip 100 Ohm termination.

Phase Shifter

Performs a fine-deskew of the output clocks and data with 260 ps (VCO @ 240 MHz) or 195 ps (VCO @ 320 MHz) steps.