Plans for Radiation Characterisation of Supported IC Technologies

CERN-PH/ESE/ME

130nm TSMC

There is no MiniASIC run in this technology. The entry price for silicon is about 45k$ (5x5mm^2)

Wafers are manufactured in 3 Fabs:
FAB14 (12 inches), FAB12 (12 inches) and FAB6 (8 inches)

	FAB14 (12 inches)	FAB12 (12 inches)	FAB6 (8 inches)
MPW/year	6	4	2
Test structures	June14	-	Sept14

Compare!

Test structures include:

	TID	DD	SEEs
Individual trans/res/FOXFET/diode	X		
Ref.Voltage Generator based on DTMOS	X	X	
Ring oscillators	X		
Shift registers (std. and HD)	X		X
Transistors for noise			

TID tests foreseen up to 400Mrad

Warning!

The plan is to rely on the natural radiation tolerance of the technology. Although unlikely for such an ‘old’ process, this could change!

1. Stay on FAB6 as much as possible for MPWs, always for dedicated runs
2. Test radiation hardness systematically on your designs
3. Drop “Standard Test Structures” in all MPW and dedicated runs if possible

65nm TSMC

MPW wafers are manufactured in 2 Fabs:
FAB14 (12 inches) and FAB12 (12 inches)

	FAB12 (12 inches)	FAB14 (12 inches)
MPW/year	6	17
Test structures	All CERN runs up to now	Fermilab chip CERN-Sept2014

From Sept2014, FAB14 is the only recommended source!

WARNING: MiniASIC runs are dispatched by IMEC on the basis of convenience to either of the two FABs!

Test structures included in Sept14 MWP

	TID	DD	SEEs	Who?
Individual trans/res/FOXFET/diode	X	X		
Individual transistors for easier study of bias influence on TID	X			
Individual transistors to assess the influence of TID/DD on mechanisms affecting reliability (NBTI, HCI, TDDB)	X	X		CERN and DEI Padova
Radiation Tolerant SRAM	X		X	CERN