Flexible Front-End Hybrids for the CMS Outer Tracker Upgrade

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On behalf of the CMS Tracker Collaboration

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Abstract

The upgrade of the CMS tracker for the HL-LHC is based on a binary readout scheme using the CMS Binary Chip (CBC2). The connectivity requirements of this flip-chip ASIC requires the use of high density interconnecting hybrids. Module integration studies indicated that a foldable flexible hybrid circuit results in an optimal module arrangement. A full module size HDI flexible hybrid was designed, integrating eight CBC2 ASICs. The hybrid is fitted with carbon fiber stiffeners and a sharp folding allows connecting the two strip sensor wirebond arrays. The front end circuit development was focused on the 2 Strip (2S) module electronics. This paper will present the implementation of the 2S front end electronics on a flexible substrate covering the mechanical and electrical properties of the assembly.

Introduction to the CMS tracker upgrade for the HL-LHC

The planned luminosity of the High Luminosity LHC (HL-LHC) requires a major upgrade of the CMS detector in order to meet the new requirements. New modules featuring higher granularity and lower mass are being developed for the upgrade. The front-end electronics of these modules will have to cope with a high data rate as a result of the increased luminosity. To reduce the amount of data forwarded in the data processing chain, the new electronics introduce the ability to correlate locally the signals from a pair of silicon sensors to enable the rejection of low momentum tracks. At the same time a new level 1 (L1) track triggering functionality is implemented to reduce the L1 trigger rate.

The CBC2 ASICs developed for these new hybrids are using flip chip technology to replace traditional wire bond connectivity to the circuit board. This type of connection allows significant size reduction and has less inductive parasitic compared to wire bonds, but it imposes the use of High Density Interconnection (HDI) technology on the front-end hybrids.

The upgrade configuration uses a barrel and endcap geometry with two different module types and sensor separations dependent on the installation region. One consists of two silicon strip sensors (2S module) with a separation of 1-4mm depending on the radial position. The other module type will consist of a silicon strip sensor and a pixelated strip sensor to provide additional Z axis information for the track triggering functionality.

The front end circuit development was focused on the 2S module electronics. This paper will present the implementation of the 2S front end electronics on a flexible substrate.

Double side strip module

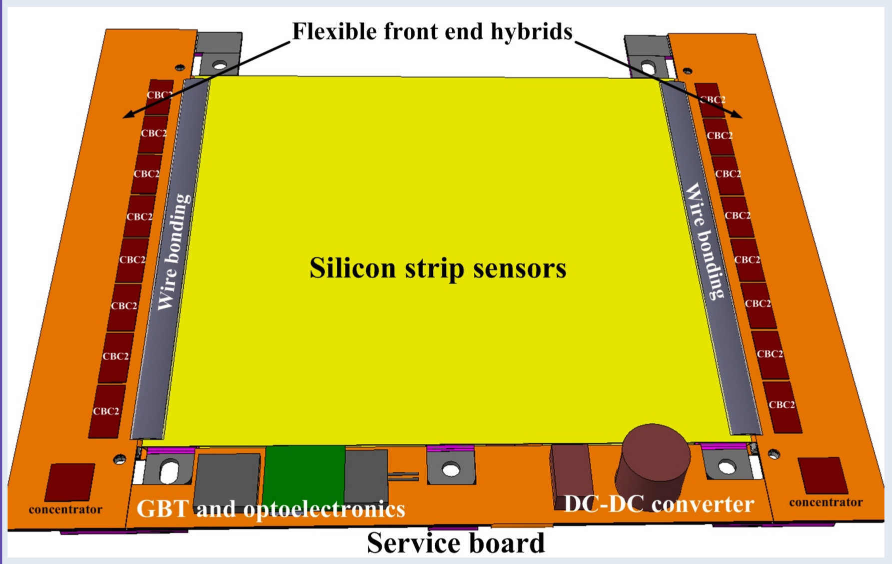

Fig.1: 2S module assembly.

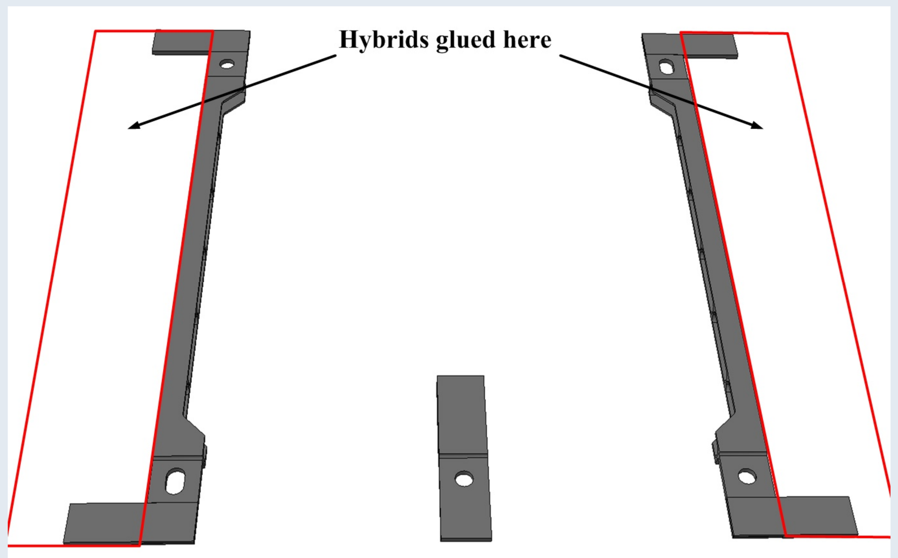

Fig.2: 2S module support and cooling.

Sensors: Each 2S module contains a pair of 100x100 mm^2 silicon strip sensors. The sensor has 1016 of parallel 50mm long strips on the two hybrid sides ending in a wire bond pad. The strips are wire bonded to the front end hybrid on both top and bottom sides.

Hybrid circuits: Two front end hybrid circuits are used in every 2S modules. Eight 2CBC ASICs are mounted on a hybrid and 127 silicon strip channels from each of the top and bottom sensors are connected to the 254 CBC2 inputs. The neighbor chips are interconnected to enable the rejection of low momentum tracks between channels located on two neighbor ASICs. A Concentrator (CIC) ASIC is connected to the digital outputs of the CBC2 chips to convert and send data towards the GBT.

Service board: A service circuit board is located between the two hybrids. The Gigabit Transmitter (GBT), opto-drivers, power connectors, DC-DC converters and a high voltage biasing circuit is fitted on this circuit board. The data and power connections are wire bonded between the service board and the hybrids.

Supporting and cooling: Three aluminum-carbon fiber composite bridges are located between the sensors to provide sufficient cooling and support for the sensors and the electronics. The electronic circuits are reinforced by carbon fiber sheets to provide stiffness and cooling.

Assembly of the CBC2 ASIC

Geometry: The CBC2 ASIC has 771 C4 bumps made of high lead Pb97Sn3 alloy in a pitch of 250 µm and the total surface area is 11.025x4.725 mm^2. The analogue inputs for the strips are located on the closest six bump rows to the wire bond pads. The digital inputs and outputs of the ASIC are well separated from the analogue inputs by several ground connections.

Routing constraints: The contact pads are solder mask defined: the solder mask opening is 125 µm of diameter and the metal pad size underneath has a diameter of 175 µm, enabling a solder mask registration error of up to ±25 µm. To avoid very narrow traces and spacing, traces are not routed between two bump pads on the top layer. To overcome this, the bumps are connected by the via in pad technology, which allows to place the via laser drill in the center of bump pads.

Under fill: To protect the bump bonding of the ASICS and to reinforce mechanically the bump assembly, an under fill material is applied between the chips and the flex circuit.

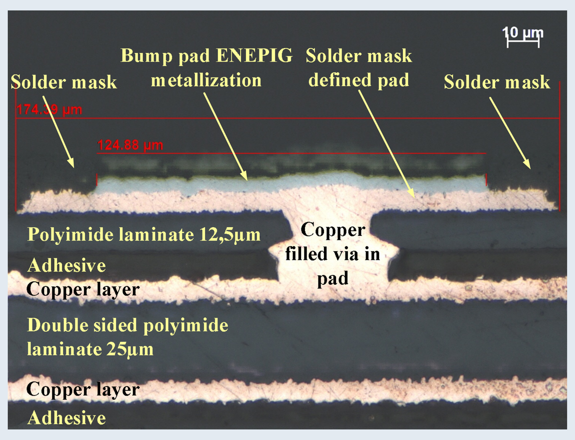

Fig.3: Copper filled via in solder mask defined pad.

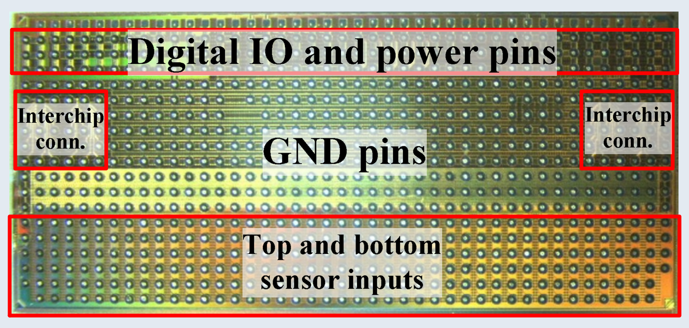

Fig.4: Functional blocks of CBC2 pins.

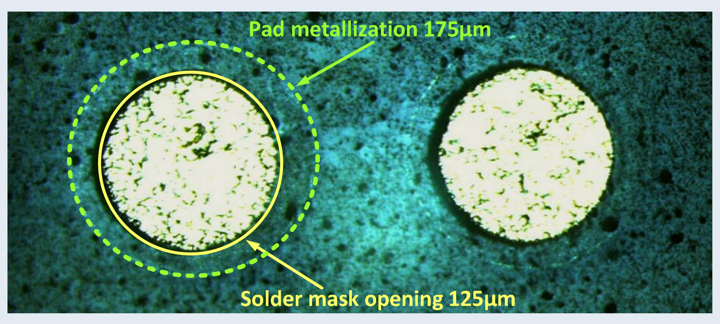

Fig.5: Solder mask defined pads on the hybrid.

Flexible front end hybrid

The full sized front end hybrid is designed to test eight CBC2 chips simultaneously with a full size silicon strip sensor. The main circuit is 125x19.5 mm^2 with two extensions, one for the wire bonds and one for a test connector. The CIC chip is missing from this prototype as the development of this ASIC is still in progress. The functionality of the CIC is implemented in the test system. The circuit is reinforced by carbon fiber stiffeners.

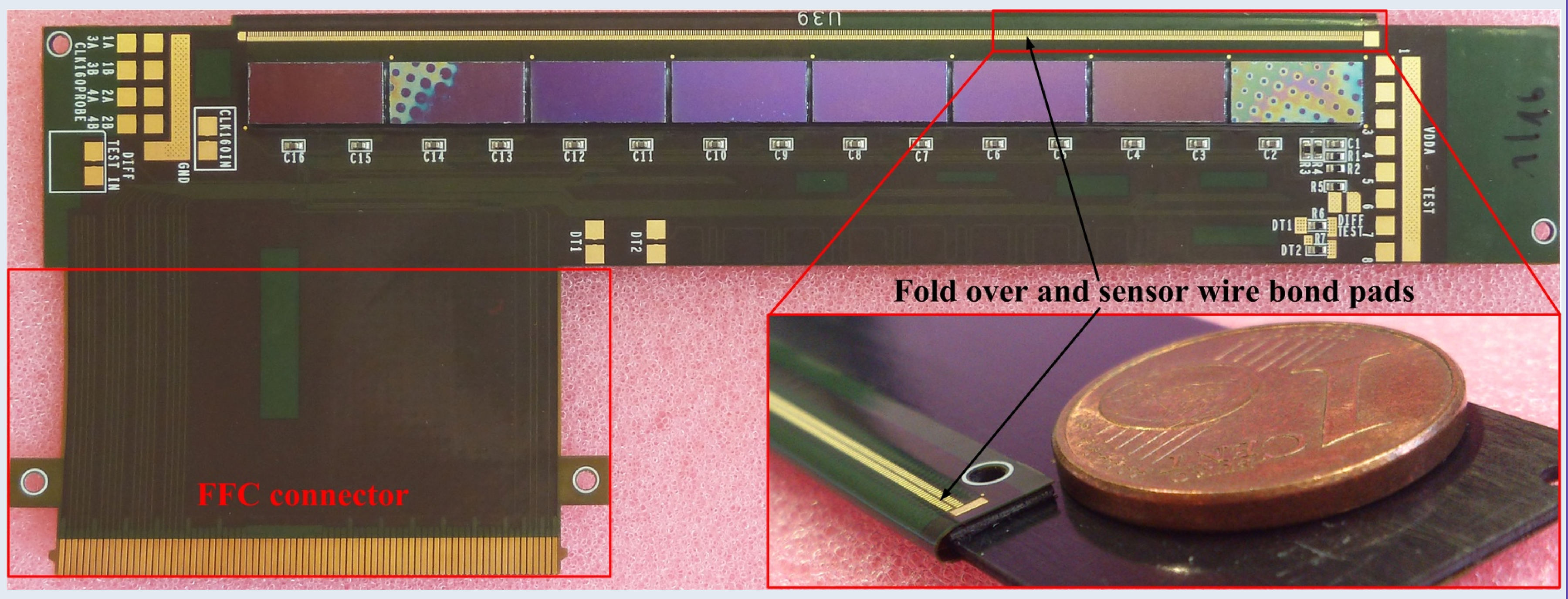

Fig.6: Front end hybrid prototype and fold over.

Build up: The circuit is using a four layers build up technology. The core layer is a double sided 25 µm polyimide laminate. The top and the bottom layers are single sided 12.5 µm polyimide laminates, glued on the core. The top layer is protected by solder mask, the bottom layer is protected by a 25 µm thick coverlay. The total thickness of the circuit is approx.: 130 µm.

HDI technology: The 90 µm strip sensor wire bonding pitch and the 250 µm pitch of the CBC2 chip are driving the constraints of the interconnection between the CBC2 chips and the sensor wire bond pads. As a result of this, the thinnest line width is 30 µm with spacing of 33 µm. The pin escapes of the flip chips are using the via in pad technology with a via capture pad size of 110 µm. The vias are copper filled with a laser drill size of 25 µm.

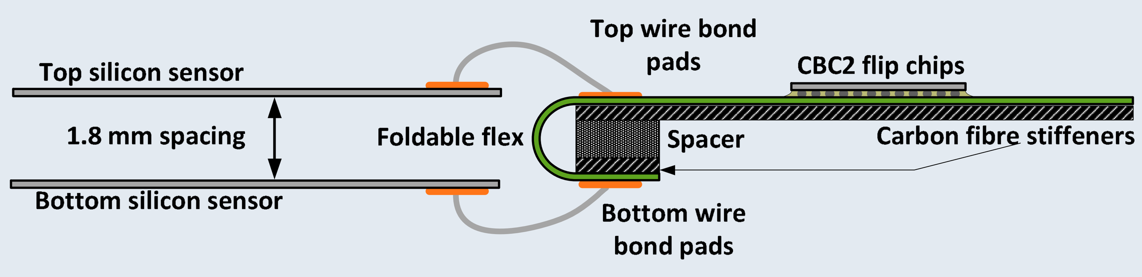

Fig.7: Fold over construction.

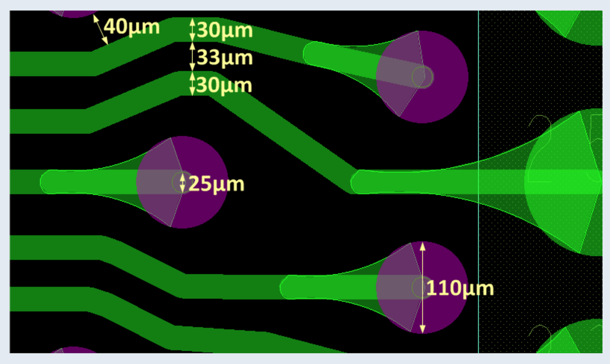

Fig.8: HDI traces and vias with tight spacing.

Fold over: The module design requires two wire bonding patterns on the top and on the bottom of the module. The bottom side wire bond pad structure is obtained by folding over the flex circuit and gluing it on a carbon fiber structure that provides a stiff wire bonding base and aligned wire bond patterns on the top and bottom sides. Additional fitting spacers can be added to match the different sensor spacings for different module types, keeping in this way the wire bonds as short as possible in all cases.

Carbon fiber stiffeners: .Two 525 µm thick carbon fiber stiffeners are glued on the circuit to provide a rigid base layer for the flip chips, the wire bond pads and the vias. On this prototype the fold over spacer material is carbon fiber as well.

Flat Flexible Connector: An FFC connector extension provides the power and data connections to the hybrid. This test extension will be removed on the final hybrid, which will be connected to the service board by wire bonds when the CIC chip will be accessible.

Test results

The hybrid is controlled and read out by a GLIB based data acquisition system through an interface card which provides power and data connectivity and signal level adapters and connected at the FFC connector.

Electrical tests are including CBC2 register programming and calibration test pulse generation to tune the comparator thresholds. S curve calibration data can then be obtained, that indicate a clean threshold transition and a uniform noise distribution across the channels. The bottom side channels exhibit a slightly higher level of noise due to the increased input capacitance caused by the longer traces connecting to the wire bond pads. Other tests included verification of correct power consumption and the probing of all wire bond pad connections to the CBC2 amplifier inputs on the hybrid.

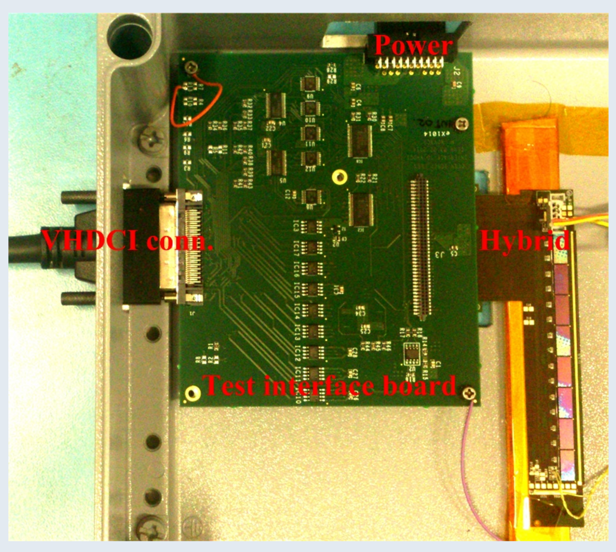

Fig.9: Hybrid connected to interface card.

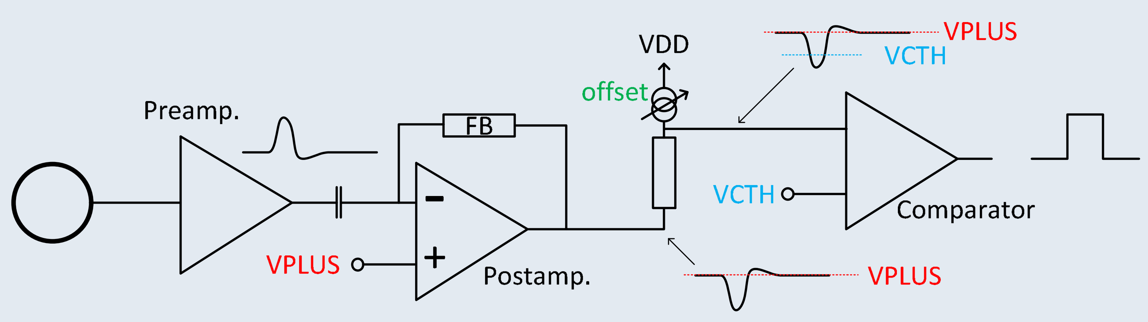

Fig.10: CBC2 analogue front end circuit.

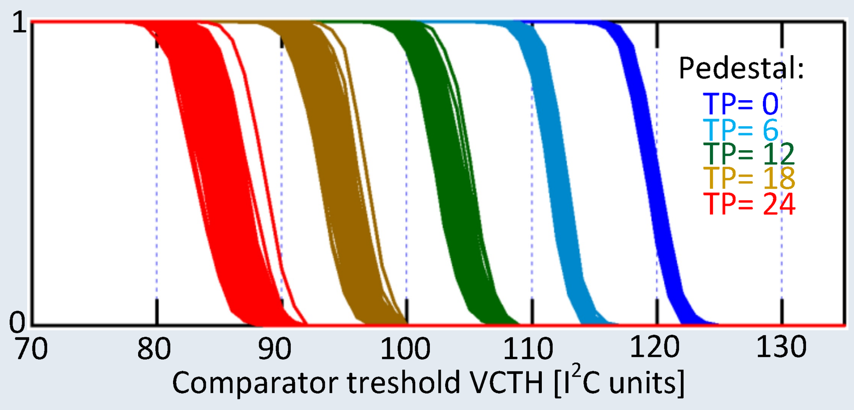

Fig.11: Raw S curve data of one CBC2 chip.

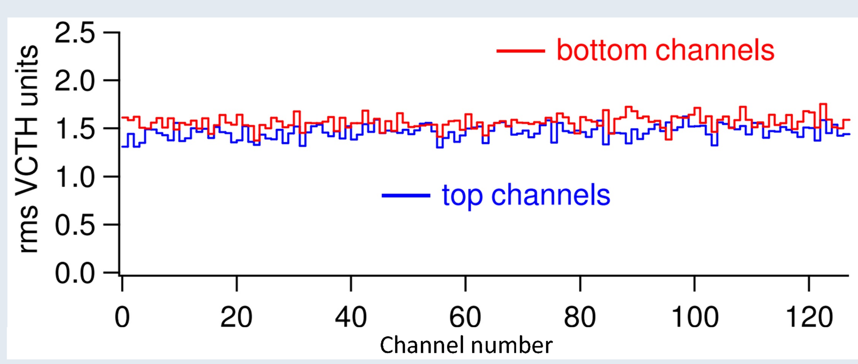

Fig.12: Noise obtained from raw S curve data.

Conclusions

A flexible front end hybrid prototype was designed and produced successfully for the 2S module. A four layer build up structure was required to route all the sensor connections to the CBC2 flip chips using HDI structures as 25 µm diameter laser drill, via in pad technology and very narrow lines and spacing. The advantage of flexibility allowed to fold down the bottom sensor wire bond pads and provided a better orientation for the wire bonding. The carbon fiber stiffeners gave sufficient rigidity for wire bonding, reinforcement for the flip chip bump bonds and kept the circuit flat and stiff, while providing a good thermal path with a minimal added mass. A test system has been developed to test the eight CBC2 chips mounted on a hybrid and to test the hybrid in the same time. Electrical tests showed that the hybrids are working as required. Further tests will be done to prove radiation hardness and long term reliability. A 2S module will be constructed as soon as the full size strip sensors become available.