ATLAS/CMS/LCD RD53 collaboration:

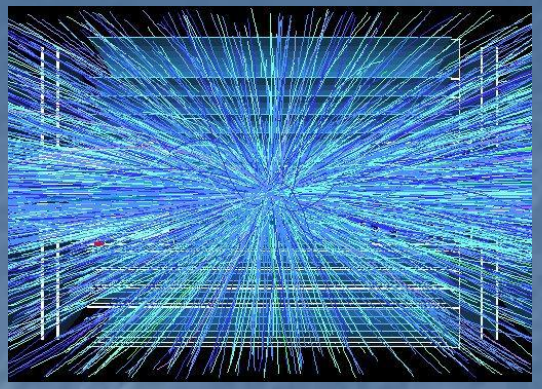
Pixel readout integrated circuits for extreme rate and radiation

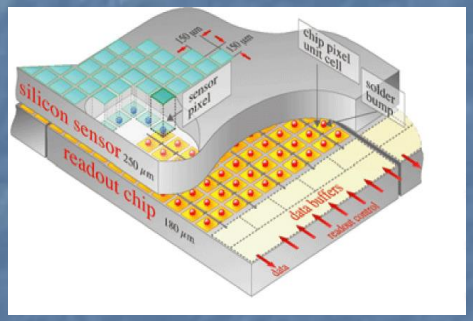
MUG at TWEPP 2014, September 2014
Jorgen Christiansen on behalf of RD53

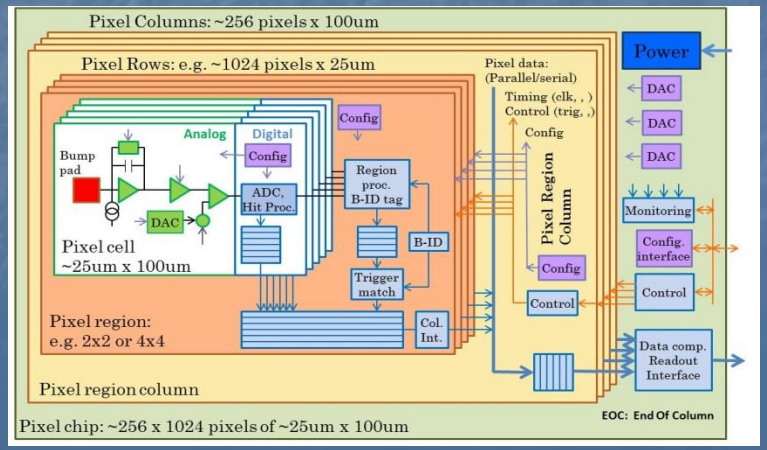
Phase 2 pixel challenges

- ATLAS and CMS phase 2 pixel upgrades very challenging
  - Very high particle rates: ~500MHz/cm^2
    - Hit rates: 2-3 GHz/cm^2 (factor ~16 higher than current pixel detectors)
  - Smaller pixels: ~¼ (50 um x 50um)
    - Increased resolution
    - Improved two track separation (jets)
  - Increased readout rates: 100kHz -> ~1MHz
    - ~100 times higher readout data rates
  - Low mass -> Low power

  Very similar requirements (and uncertainties) for ATLAS & CMS
- Unprecedented hostile radiation: 1Grad, 10^{16} Neu/cm^2
  - Hybrid pixel detector with separate readout chip and sensor.
  - Phase2 pixel will get in 1 year what we now get in 10 years
- Pixel sensor(s) not yet determined
  - Planar, 3D, Diamond, HV CMOS, , ,
  - Possibility of using different sensors in different layers
  - Final sensor decision may come relatively late.
- Very complex, high rate and radiation hard pixel readout chips required







RD53 in a nutshell

- Focussed R&D program to develop pixel chips for ATLAS/CMS phase 2 upgrades and LCD vertex
- RD53 collaboration: 19 institutes, ~100 people
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, PSI, RAL, Torino, UC Santa Cruz.
- Extremely challenging requirements (ATLAS/CMS):
  - Small pixels: $50x50um^2$ ($25x100um^2$)
    Support for larger pixels (50x100, 100x100, ,)
  - Large chips: ~2cm x 2cm (~1 billion transistors)
  - Hit rates: ~2 GHz/cm^2
  - Radiation: 1Grad, 10^{16} neu/cm^2 (unprecedented)
  - Trigger: ~1MHz, 10-20us (~100x buffering and readout)
  - Low power - Low mass systems
- Baseline technology: 65nm CMOS
- Full scale demonstrator pixel chip in 3 year R&D program

Working groups

WG	Domain
WG1	Radiation test/qualification
Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm	
WG2	Top level
Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.	
WG3	Simulation/verification framework
System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells	
WG4	I/O
Development of rad hard IO cells Standardized interfaces: Control, Readout, etc.	
WG5	Analog design / analog front-end
Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends	
WG6	IP blocks
Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation	

Radiation WG

- Radiation test and qualification 65nm: 1Grad and 10^{16} neu/cm^2
- WG convener: Marlon Barbero, CPPM
- Activities and Status:
  - Defining radiation testing procedure: X-ray, Cobalt source, Proton linac
  - Test of 65nm transistors to 1Grad
    - **NMOS: Acceptable degradation**
    - **PMOS: Severe radiation damage above 300Mrad** (next slide)
      - Not yet a clear understanding of effects seen at these unprecedented radiation levels
      - ESD damage from manipulation and test systems ?
      - **Much less radiation degradation when radiated cold (-25°C): Unexpected. Annealing effects to be verified.**
    - Systematic radiation/annealing studies required to be verified with pixel detector operation (cold -20°C)
  - Test of circuits to 1Grad
    - Ring oscillators, Pixel chips (CERN, LBNL)
    - Some digital circuits remains operational up to 1Grad, depending on digital library used. (better than indicated by tests of individual transistors)

Critical to confirm if 65nm is OK for inner layers of pixel detectors

- Alternative foundries/technologies or replacement of inner layers after a few years ?

More on this in plenary talk tomorrow morning

- Plans
  - Systematic radiation and annealing studies of 65nm basic devices and circuits including cold radiation
  - Hadron/neutron radiation tests for NIEL effects
  - Radiation test of basic transistors/structures in alternative technologies (for comparison/understanding)
  - Simulation models of radiation degraded transistors (if possible)
- CERN, CPPM, Fermilab, LBNL, New mexico, Padova

IP WG

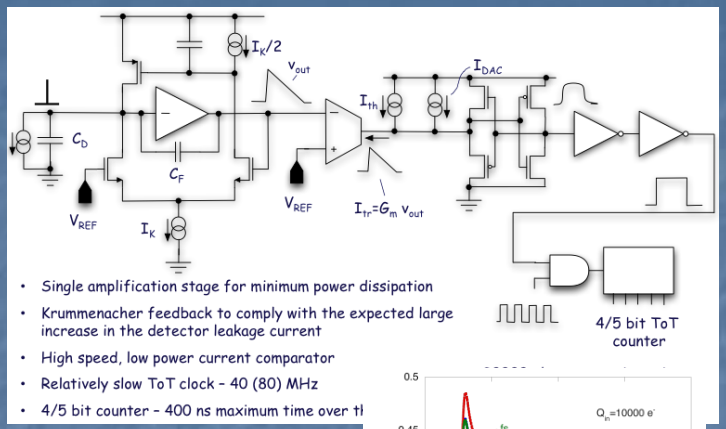
- IP blocks required to build pixel chips
- Convener: Jorgen Christiansen, CERN
- Activities and status
  - List of required IPs (30) defined and assigned to groups
    - IP specs reviewed July 2014. Recommendations for rad hard design.
  - Defining how to make IPs appropriate for integration into mixed signal design flow for full/final pixel chips
    - IP expert panel
    - CERN design flow
  - Design of IP blocks have started
- Plans
  - Recommendations for IP design for pixel chip and radiation hardness
  - Common IP/design repository
  - Prototyping/test: 2014/2015
  - IP blocks ready 2015/2016
- ~All RD53 institutes

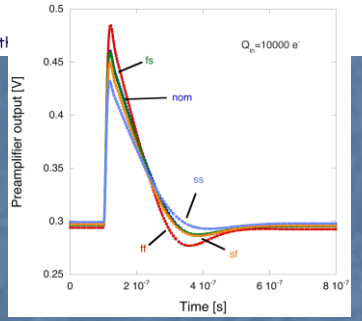
Country	DE		FR	NL		IT - INFN			US	FR	UK	US	CZ	Comments	Contacts
Group	Bonn	CERN	CPPM	NIKHEF	Bari/Pav/Berg	Milano	Padova	Pisa	Torino	LBNL	LPNHE	RAL/Sanfo	Cruz	Prague		
ANALOG: Coordination with analog WG																
Temperature sensor.			O		(P)			(P)						(P)		CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
Radiation sensor			O		(P)			(P)						(P)		CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
HV leakage current sensor.			O					(P)						(P)		CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
Band gap reference		O	O	(P)	O						(P)				3 Groups	Pavia/Bergamo: Gianluca Traversi, gianluca.traversi@unibg.it CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr CERN: Stefano Michelis, Stefano.Michelis@cern.ch NIKHEF: Vladimir Gromov , vgromov@nikhef.nl
Self-biased Rail to Rail analog buffer	(P)		(P)	(P)							O			(P)		RAL: Steve Thomas, stephen.thomas@stfc.ac.uk NIKHEF: Vladimir Gromov , vgromov@nikhef.nl
MIXED																
8 – 12 bit biasing DAC		(P)			O									O	2 groups	Bari: Flavio Loddo, flavio.loddo@ba.infn.it Prague: Gordon Neue, Gordon.Neue@fjfi.cvut.cz
10 - 12 bit slow ADC for monitoring		O	O		O										3 Groups	Bari: Cristoforo Marzocca, marzocca@poliba.it CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr; CERN: Sandro Bonacini, sandro. bonacini@cern.ch
PLL for clock multiplication	O	(P)		(P)			(P)	(P)	(P)		(P)	(P)			Together	Bonn: Hans Kruger, krueger@physik.uni-bonn.de (NIKHEF: Vladimir Gromov , vgromov@nikhef.nl)
High speed serializer (~Gbit/s)	O	(P)		(P)				(P)			(P)	(P)				Bonn: Hans Kruger, krueger@physik.uni-bonn.de (NIKHEF: Vladimir Gromov , vgromov@nikhef.nl)
(Voltage controlled Oscillator)				(P)			O	(P)	(P)						Needed ?	Padova: Daniele Vogrig, vogrig@dei.unipd.it (Pisa: Guido Magazzu, Guido.Magazzu@cern.ch) (NIKHEF: Vladimir Gromov , vgromov@nikhef.nl)
Clock recovery and jitter filter	O	(P)						(P)			(P)					Bonn: Hans Kruger, krueger@physik.uni-bonn.de
Programmable delay	O	(P)						(P)			(P)					Bonn: Hans Kruger, krueger@physik.uni-bonn.de
DIGITAL																
SRAM for pixel region	(P)	(P)				O						(P)				Milano: Seyedruhollah Shojaii, Seyedruhollah.shojaii@cern.ch
SRAM/FIFO for EOC.	(P)	(P)				(P)		(P)				O				Santa Cruz: Joel DeWitt, joel_dewitt@sbcglobal.net
EPROM/EFUSE	(P)	O	(P)													
DICE storage cell / config reg	(P)		O			(P)		(P)				(P)			Or TMR ?	CPPM: Mohsine Menouni, menouni@cppm.in2p3.fr
LP Clock driver/receiver	(P)				O						(P)					Pavia/Bergamo: Gianluca Traversi, gianluca.traversi@unibg.it
(Dedicated rad hard digital library)	(P)	(P)	(P)					O		(P)	(P)				If needed	Pisa: Fabio Morsani, fabio.morsani@pi.infn.it
(compact mini digital library for pixels)	(P)	(P)	(P)					O		(P)	(P)				If needed	Pisa: Fabio Morsani, fabio.morsani@pi.infn.it
IO: Coordination with IO WG																
Basic IO cells for radiation	(P)	O														CERN: Sandro Bonacini, sandro.bonacini@cern.ch
Low speed SLVS driver (<100MHz)	(P)	(P)			O			(P)	(P)					(P)		Pavia/Bergamo: Gianluca Traversi, gianluca.traversi@unibg.it (Pisa: Guido Magazzu, Guido.Magazzu@cern.ch)
High speed SLVS driver (~1Gbits/s)	(P)	(P)			O			(P)	(P)					(P)	Together	Pavia/Bergamo: Gianluca Traversi, gianluca.traversi@unibg.it (Pisa: Guido Magazzu, Guido.Magazzu@cern.ch)
SLVS receiver	(P)	(P)			O			(P)						(P)		Pavia/Bergamo: Gianluca Traversi, gianluca.traversi@unibg.it
1Gbits/s drv/reccable equalizer															New	
C4 and wire bond pads	(P)	O														
(IO pad for TSV)	O		(P)								(P)		(P)		(If needed)	Bonn: Hans Kruger, krueger@physik.uni-bonn.de
Analog Rail to Rail output buffer	O		(P)								(P)		(P)			Bonn: Hans Kruger, krueger@physik.uni-bonn.de
Analog input pad	O										(P)					Bonn: Hans Kruger, krueger@physik.uni-bonn.de
POWER																
LDO(s)	O	(P)	(P)	(P)				(P)	(P)		(P)					Bonn: Michael Karagounis, michael.karagounis@hshl.de (NIKHEF: Deepak Gajanana, deepakg@nikhef.nl)
Switched capacitor DC/DC		(P)								O				(P)		LBNL: Maurice Garcia-Sciveres, mgarcia-sciveres@lbl.gov
Shunt regulator for serial powering	O			(P)												Bonn: Michael Karagounis, michael.karagounis@hshl.de (NIKHEF: Deepak Gajanana, deepakg@nikhef.nl)
Power-on reset															New	
Power pads with appropriate ESD	(P)	O														CERN: Sandro Bonacini, sandro.bonacini@cern.ch
SOFT IP: Coordination with IO WG																
Control and command interface		(P)			(P)			O			(P)					Pisa: Roberto Beccherle, Roberto.Beccherle@cern.ch
Readout interface (E-link ?)		(P)			(P)			O			(P)					Pisa: Roberto Beccherle, Roberto.Beccherle@cern.ch

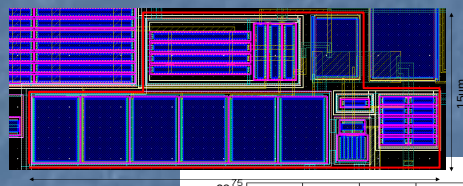
Analog WG

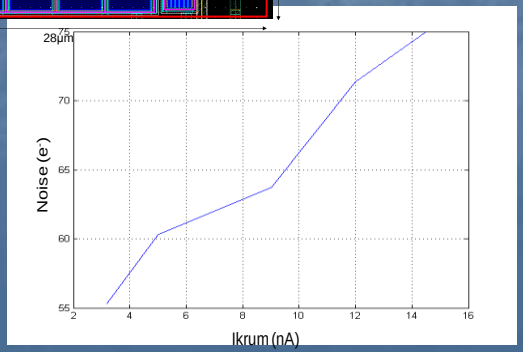
- Evaluation, design and test of appropriate low power analog pixel Front-Ends
- Convener: Valerio Re, Bergamo/Pavia
- Activities and status
  - Analog front-end specifications
    - Planar, 3D sensors, capacitance, threshold, charge resolution, noise, deadtime, ,
  - Alternative architectures –implementations to be compared, designed and tested by different groups
    - TOT, ADC, Synchronous, Asynchronous, Threshold adjust, Auto zeroing, etc.
  - Design / prototyping of FE's ongoing
- Plans
  - Prototyping and test (with radiation) different FEs
    - Some FEs have already been prototyped
    - Others will be prototyped after the summer
  - Test, comparison and choice of most appropriate FE(s)
- Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, Prague IP/FNSPE-CTU, Torino.

Krummenacher – TOT examples



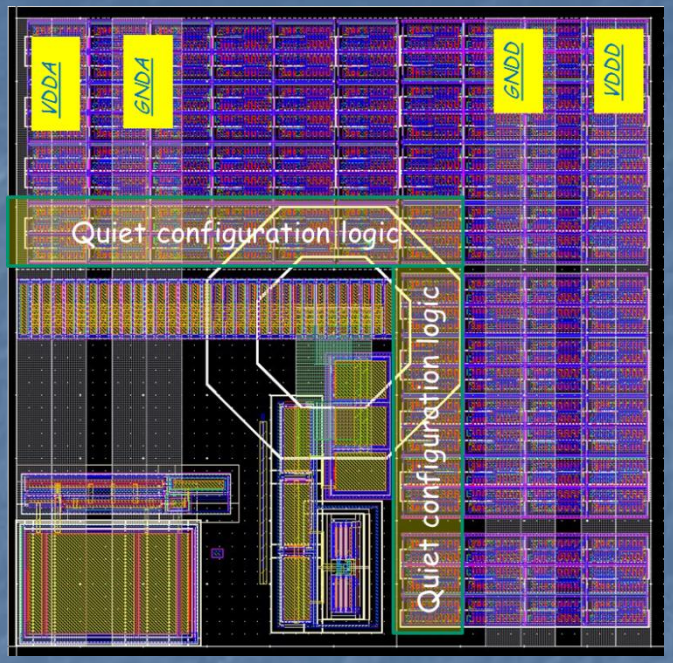


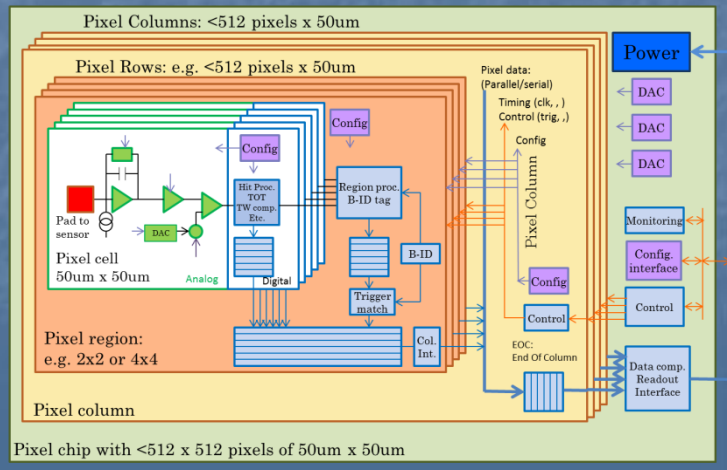




Top level WG

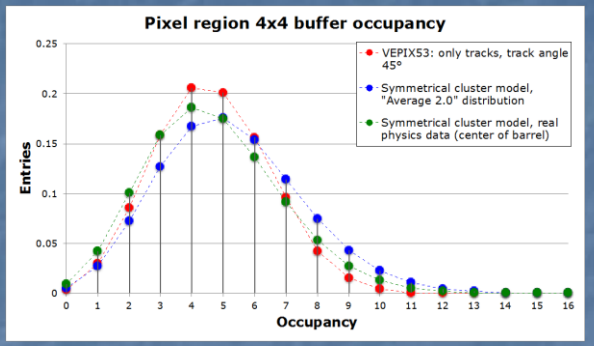
- Global architecture and floor-plan issues for large mixed signal pixel chip
- Convener: Maurice Garcia-Sciveres, LBNL
- Activities and status
  - Global floorplan issues for pixel matrix
    - 50x50um^2 – 25x100um^2 pixels with same pixel chip
      - ATLAS – CMS has agreed to initially aim for this
    - Compatibility with bigger pixels for outer layers
    - Global floor-plan with analog and digital regions
  - Appropriate design flow
  - Column data bus versus serial links
  - Simplified matrix structure for initial pixel array test chips
- Plans
  - Submission of common simplified pixel matrix test chips
  - Evaluation of different pixel chip (digital) architectures
    - Using simulation frameworks from simulation WG.
  - Final integration of full pixel chip
- Bonn, LBNL, , , ,



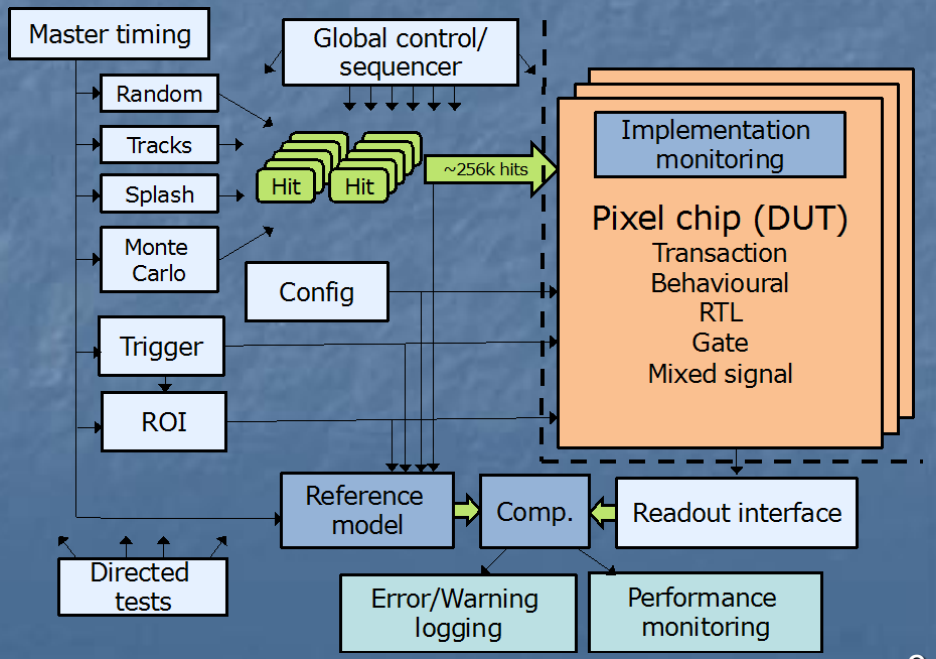


Simulation/verification WG

- Simulation and verification framework for complex pixel chips
- Convener: Tomasz Hemperek, Bonn
- Activities and status
  - Simulation framework based on system Verilog and UVM (industry standard for ASIC design and verification)
    - High abstraction level down to detailed gate/transistor level
    - Benchmarked using FEI4 design
  - First basic version of framework available on common repository
    - Internal generation of appropriate hit patterns
    - Used for initial study of buffering architectures in pixel array
  - Integration with ROOT to import hits from detector simulations and for monitoring and analysing results.
- Plans
  - Refine/finalize framework with detailed reference model of pixel chip
  - Import pixel hit patterns from detector Monte-Carlo simulation
  - Modelling of different pixel chip architectures and optimization
  - Verification of final pixel chip
- Bonn, CERN, Perugia



Buffer occupancy comparison between simulation and analytical statistical model



IO WG

- Defining and implementing readout and control interfaces
  - Common test interfaces and test hardware
- Convener: Roberto Beccherle, Pisa (just assigned)
- Plans
  - Defining readout and control protocols
  - Implement/verify IO blocks for pixel chip
  - Standardized pixel test systems
- Pisa, Bonn , , ,

RD53 Outlook

- 2014:
  - Release of CERN 65nm design kit. RD53 eagerly awaiting this (NDA issues).
  - **Detailed understanding of radiation effects in 65nm**
    - Cold operation
    - Radiation test of few alternative technologies.
    - Spice models of transistors after radiation/annealing
  - **IP/FE block responsibilities defined** and appearance of first FE and IP designs/prototypes
  - Simulation framework with realistic hit generation and auto-verification.
  - Alternative architectures defined and efforts to simulate and compare these defined
  - **Common MPW submission 1**: First versions of IP blocks and analog FEs
- 2015:
  - Common MPW submission 2: Near final versions of IP blocks and FEs.
  - Final versions of IP blocks and FEs: Tested prototypes, documentation, simulation, etc.
  - IO interface of pixel chip defined in detail
  - **Global architecture defined and extensively simulated**
  - **Common MPW submission 3: Final IPs and FEs, Initial pixel array(s)**
- 2016:
  - **Common engineering run: Full sized pixel array chip**.
  - Pixel chip tests, radiation tests, beam tests , ,
- 2017:
  - Separate or common ATLAS – CMS final pixel chip submissions.

RD53 Summary

- RD53 has gotten a good start
  - Organization structure put in place
  - Technical work in WGs have started

  Significant organisational effort.
- Radiation tolerance of 65nm remains critical
  - Design work has started in 65nm (FEs, IPs)
  - Radiated cold, Annealing effects/scenario to be understood
  - Backup: Inner layer replacement versus alternative technology
- RD53 is a recognized collaboration reporting in relevant HEP/pixel meetings:
  - ATLAS/CMS meetings
  - LHCC: http://indico.cern.ch/event/319702/session/1/contribution/36/material/slides/0.pptx
  - ACES2014: https://aces.web.cern.ch/aces/aces2014/ACES2014.htm
  - Front-end electronics workshop: http://indico.cern.ch/event/276611/overview
  - Pixel: https://indico.cern.ch/event/302139/session/14/contribution/175/material/slides/0.pdf
  - Vertex: https://indico.cern.ch/event/300851/session/8/contribution/45/material/slides/0.pptx
  - TWEPP: https://indico.cern.ch/event/299180/session/25/contribution/110
- Funding for RD53 work starts to materialize in institutes
- CMS and ATLAS relies on RD53 for their pixel upgrades

Access to RD53 information

- Access to RD53 meetings and documents by default limited to RD53 members.
- Special "RD53 guests" category that can get full access to meetings and documents:
  - Members of ATLAS/CMS pixel upgrade projects
  - Institutes requesting to become active RD53 members.
  - CERN 65nm technology support
  - Others when well justified.

Backup slides

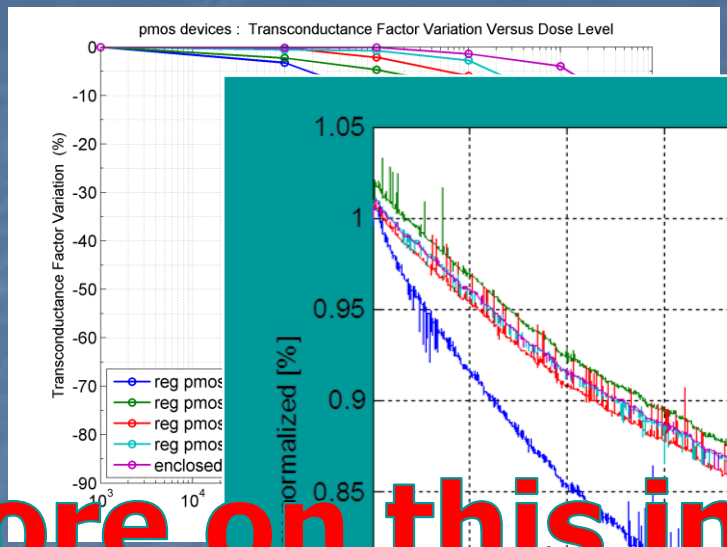
ATLAS – CMS RD collaboration

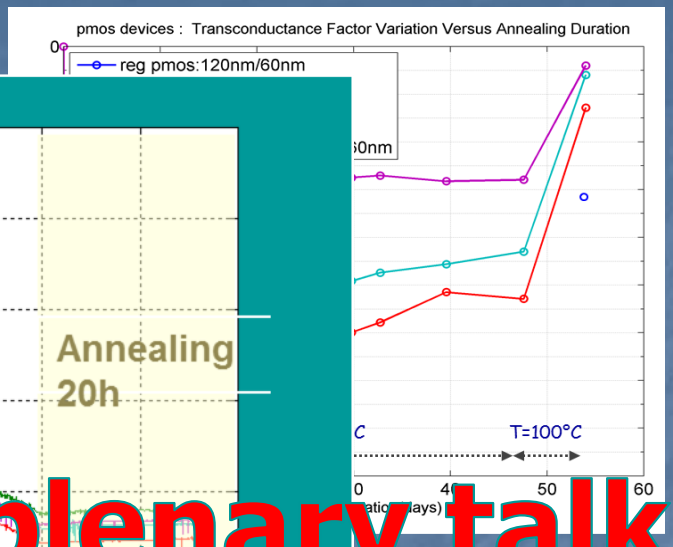
- Similar/identical requirements, same technology choice and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS – ATLAS RD collaboration
  - Even if we do not make a common pixel chip
- Initial 2day workshop between communities confirmed this.
  - Workshop: http://indico.cern.ch/conferenceDisplay.py?confId=208595
- Forming a RD collaboration has attracted additional groups and collaborators
  - Synergy with CLIC pixel (and others): Technology, Rad tol, Tools, etc.
- Institutes: 17
  - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, RAL, UC Santa Cruz.
  - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino.
- Collaborators: 99, ~50% chip designers
- Collaboration organized by Institute Board (IB) with technical work done in specialized Working Groups (WG)
- Initial work program covers ~3 years to make foundation for final pixel chips
  - Will be extended if appropriate:
    A. Common design ?,
    B. Support to experiment specific designs

Organisation issues

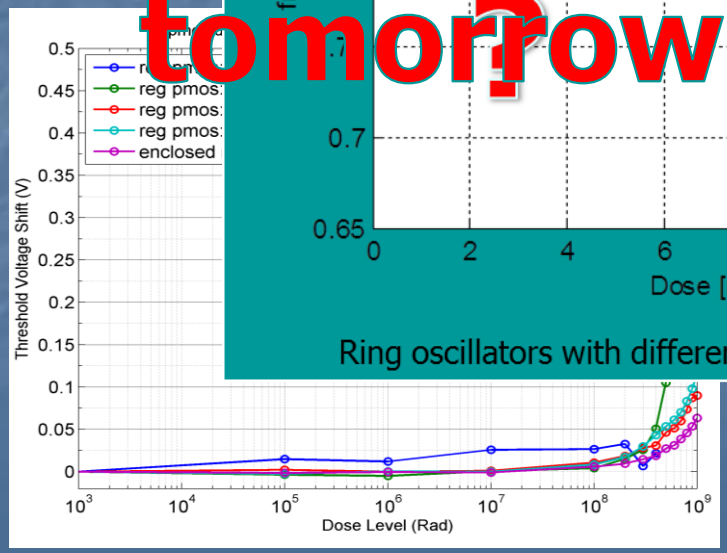
- 19 Institutes (2 new institutes have joined)
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, **Milano**, NIKHEF, New Mexico, Padova, Perugia, Pisa, **Prague IP/FNSPE-CTU**, PSI, RAL, Torino, UC Santa Cruz.
  - ~100 collaborators
  - 2 institutes requesting to join: LAL/OMEGA, Seville
- Spokes persons: Maurice Garcia-Sciveres, LBNL (ATLAS), Jorgen Christiansen, CERN (CMS)
  - 2 year terms
- Institute Board
  - IB chair: Lino Demaria, Torino
  - Regular IB meetings
  - MOU drafted and ready to be signed
- Management board: Spokes persons, IB chair, WG conveners
  - Monthly meetings
- Mailing lists, INDICO, CDS, TWIKI: http://twiki.cern.ch/RD53 , etc. set up
- Technical Working Groups have started
  - WG conveners
  - Regular WG meetings
- RD53 collaboration meetings:
  - pre-RD53 meeting in Nov. 2012
  - CERN April 10-11, 2014. 64 participants: https://indico.cern.ch/event/296570
  - RAL Oct. 16-17, 2014

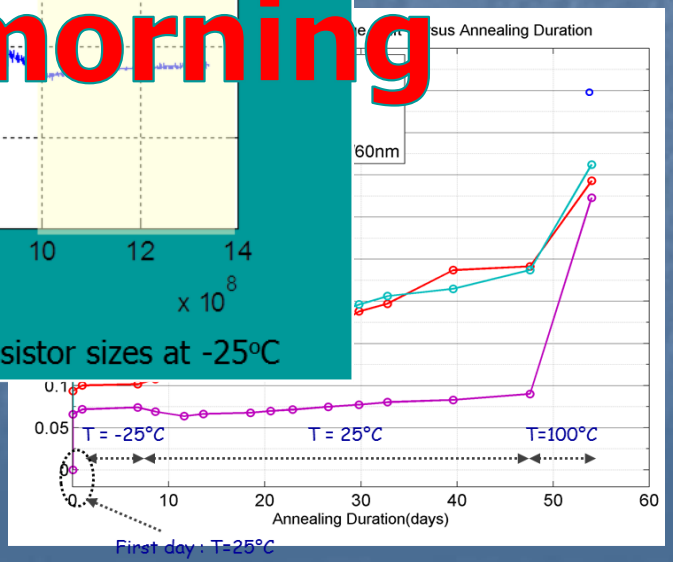
PMOS Radiation effects 65nm





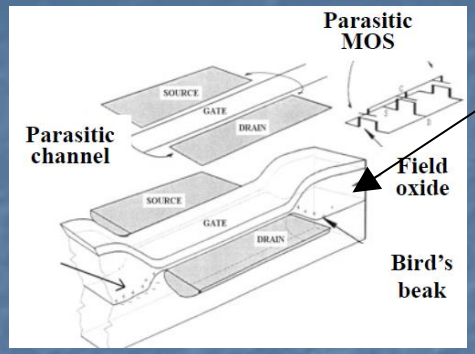
More on this in plenary talk tomorrow morning





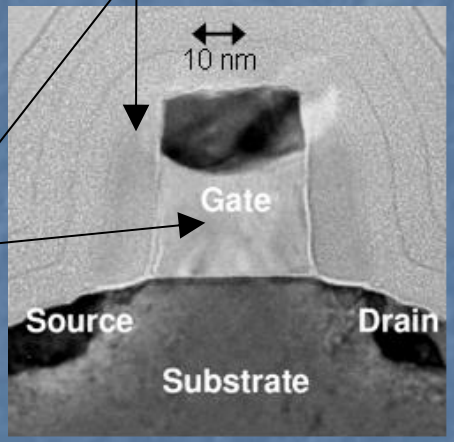
Vt shift

Radiation effects



Birds beak parasitic device

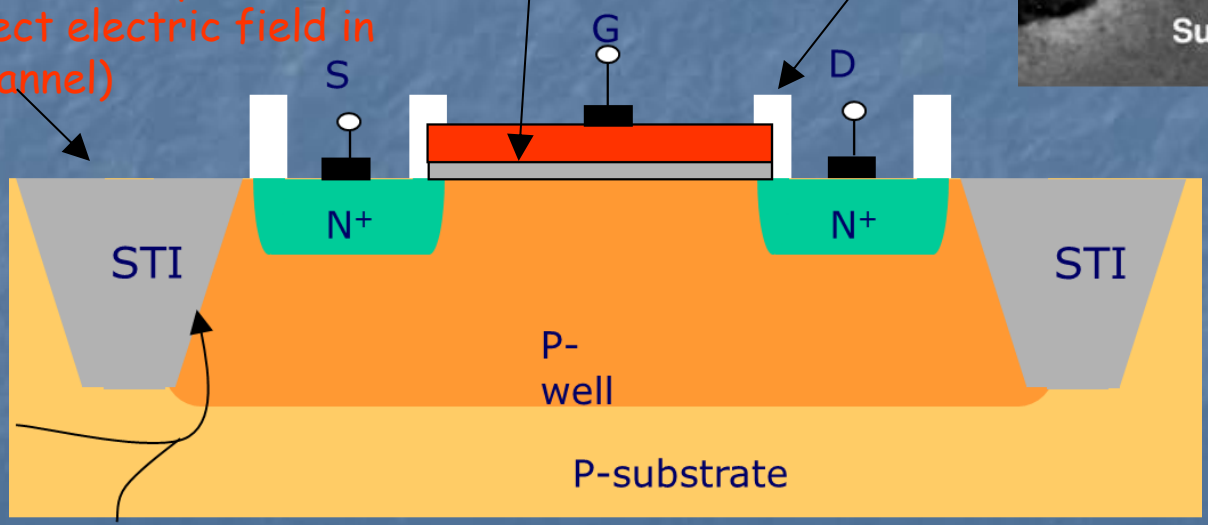
Spacer dielectrics may be radiation-sensitive



Charge buildup in gate oxide and interface states affects Vt

Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

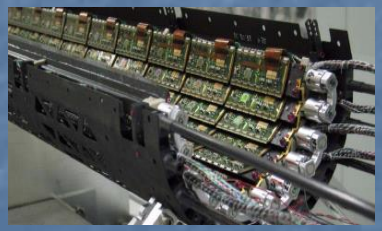
Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices

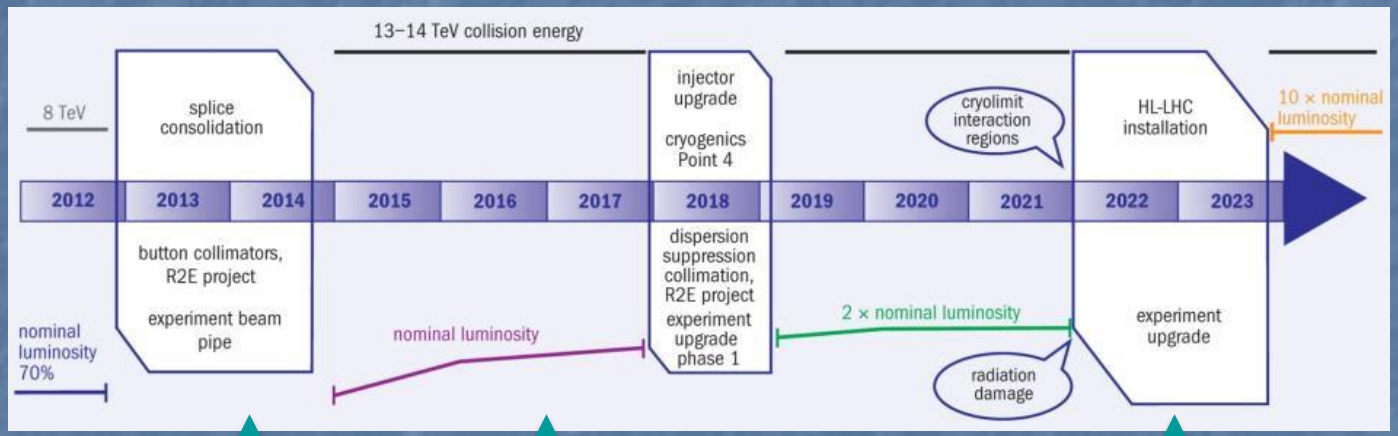


Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

Pixel upgrades

- Current LHC pixel detectors have clearly demonstrated the feasibility and power of pixel detectors for tracking in high rate environments
- Phase1 upgrades: Additional pixel layer, ~4 x hit rates
  - ATLAS: Addition of inner B layer with new 130nm pixel ASIC (FEI4)
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG)
- **Phase2 upgrades**: ~16 x hit rates, 2-4 x better resolution, 10 x readout rates, 16 x radiation tolerance, Increased forward coverage, less material, , ,
  - Installation: ~ 2022
  - Relies fully on significantly improved performance from next generation pixel chips.





ATLAS Pixel IBL

CMS Pixel phase1

CMS & ATLAS phase 2 pixel upgrades

100MHz/cm^2

400MHz/cm^2

1-2GHz/cm^2

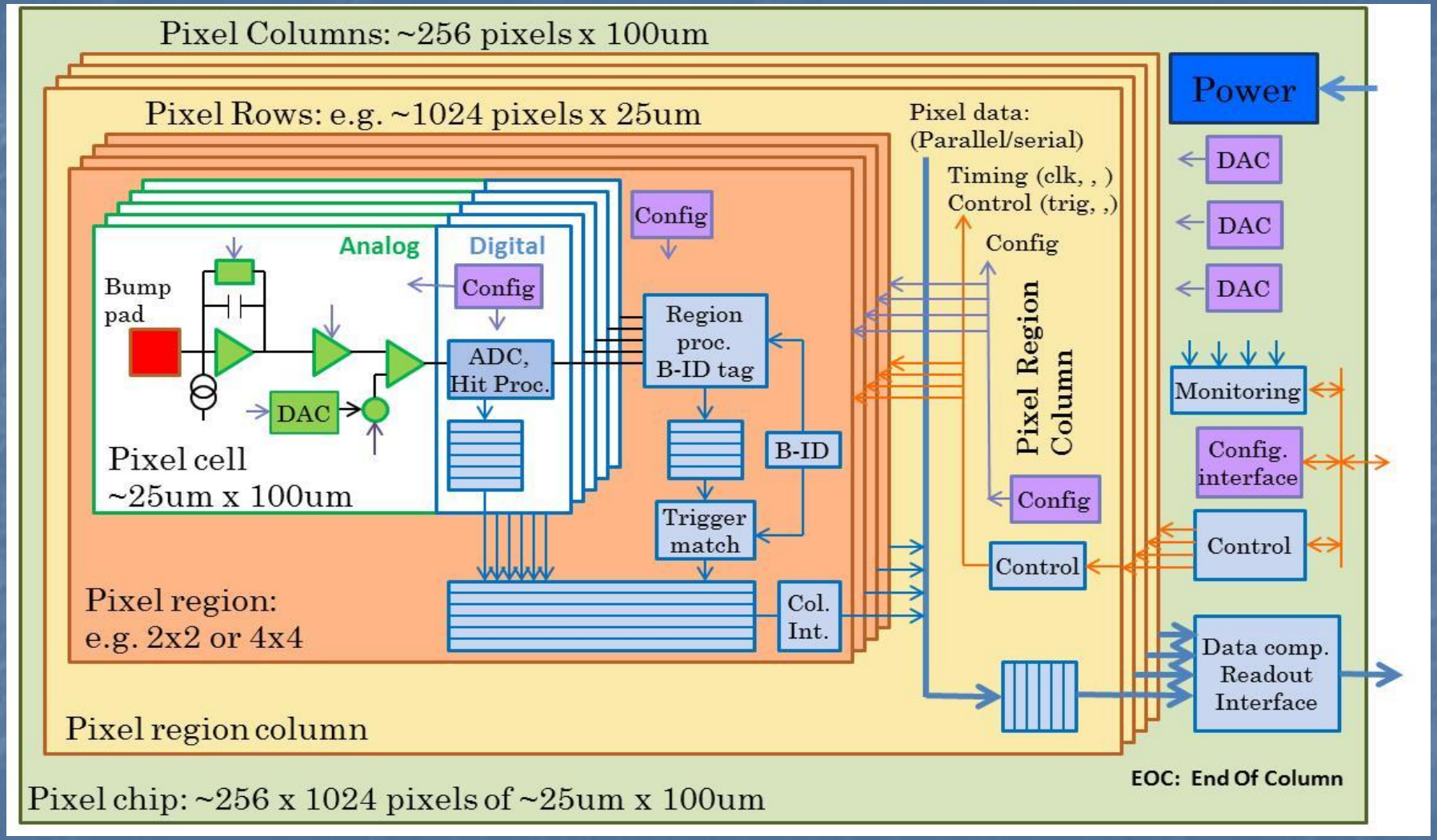
Pixel chip

- Pixel readout chips critical for schedule to be ready for phase 2 upgrades
  - Technology: Radiation qualification
  - Building blocks: Design, prototyping and test
  - Architecture definition/optimization/verification
  - Chip prototyping, iterations, test, qualification and production
  - System integration
    - System integration tests and test-beams
  - Production and final system integration, test and commissioning
- Phase 2 pixel chip very challenging
  - Radiation
  - Reliability: Several storage nodes will have SEUs every second per chip.
  - High rates
  - Mixed signal with very tight integration of analog and digital
  - Complex: ~256k channel DAQ system on a single chip
  - Large chip: ~2cm x 2cm, ½ - 1 Billion transistors.
  - Very low power: Low power design and on chip power conversion
- Both experiments have evolved to have similar pixel chip architectures and plans to use same technology for its implementation.
- Experienced chip designers for complex ICs in modern technologies that most work in a extremely harsh radiation environment is a scarce and distributed "resource" in HEP.

Pixel chip generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2
Pixel size	100x150um^2 (CMS) 50x400um^2 (ATLAS)	100x150um^2 (CMS) 50x250um^2 (ATLAS)	25x100um^2 ?
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, MAPS ?
Chip size	7.5x10.5mm^2 (ATLAS) 8x10mm^2 (CMS)	20x20mm^2 (ATLAS) 8x10mm^2 (CMS)	**> 20 x 20mm^2**
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	**~1G**
Hit rate	**100MHz/cm^2**	**400MHz/cm^2**	**1-2 GHz/cm^2**
Hit memory per chip	0.1Mb	1Mb	~16Mb
Trigger rate	100kHz	100KHz	200kHz - **1MHz**
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	6 - 20us
Readout rate	40Mb/s	320Mb/s	**1-3Gb/s**
Radiation	**100Mrad**	**200Mrad**	**1Grad**
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	**65nm**
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	Digital
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	Pixel
Power	~1/4 W/cm^2	~1/4 W/cm^2	**~1/4 W/cm^2**

3rd generation pixel architecture



- 95% digital (as FEI4)
- Charge digitization
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column

IP Schedule

- ~2 years to make IPs.
  To have full pixel array ROC at end of 3 year RD53 program
  - Who makes what and how: Done
  - Specs of each IP: NOW
  - Viable schematic/layout: Q4 2014
  - Prototype submission: Q1 2015 (shared MPW)
  - Behavioural model Q2 2015 (to allow progress on global pixel)
  - Tested Prototype: Q3 2015
  - Radiation qualification: Q4 2015
  - (2^{nd}. Prototype) Q4 2015 (shared MPW submission)
  - Final IP: Q1 2016
    - Long list of things to deliver for each IP