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Active Pixel Sensors for the ATLAS Upgrade - Concepts and Test Chip Results

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We explore the concept of using deep-submicron HV-CMOS and/or imaging processes to produce a drop-in replacement for radiation-hard silicon sensors. Such active sensors contain simple circuits, e.g. amplifiers and discriminators, but still require a readout chip. This approach yields most advantages of MAPS, without the complication of full integration on a single chip.
After outlining the basic concept and the design of recent test ASICs, characterization results after irradiation up to 1e16 neq/cm2 and 1GRad will be presented, and future plans with active sensors for the ATLAS Upgrade will be discussed.

Summary

Deep-submicron HV-CMOS processes feature moderate bulk resistivity and HV capability and are therefore good candidates for drift-based radiation-hard monolithic active pixel sensors (MAPS). It is possible to apply 60-100V of bias voltage leading to a depletion depth of ˜10-20 um. Thanks to the high electric field, charge collection is fast and nearly insensitive to radiation-induced trapping. CMOS Imaging Processes often feature high-resistive substrates, thinning, stitching and backside processing, which makes them also interesting to study.

We explore the concept of using such processes to produce active pixel sensors (APS) that contain simple circuits to amplify and discriminate the signal. A readout chip (ROC) is still needed to receive and organize the data from the active sensor and handle high-level functionality such as trigger management. This chip can follow the pixel chip concept with the readout circuits distributed over the area of the chip, or the strip concept with one or few rows of pads along one (or more) sides of the chip. The connection between APS and ROC can be made in a “traditional”way (wire/bump-bonding) or by capacitive coupling (e.g. gluing) which could lower the production cost significantly.

The active sensor approach offers many advantages with respect to standard silicon sensors: fabrication in commercial CMOS processes costs less than traditional diode sensors, aggressive thinning is resulting in much lower mass, bias voltage and operation temperature requirements are favorable. From a practical perspective, maintaining the traditional separation between sensing and processing functions lowers development cost and makes use of existing infrastructure.

ATLAS-compatible test ASICs were produced in a variety of processes. Either strip-like or pixel-like readout could be selected on the most devices. Typical sub-pixel sizes amount to 33 by 125 um which are multiplexed into FE-I4-like pixels using pulse-height-encoding to encode the position of the hit sub-pixel. They were capacitively coupled by gluing with less than about 10 µm of glue layer thickness. For strip readout, the position along the virtual strip was pulse-height-encoded, too. First results of their characterization, partially also after irradiation to HL-LHC fluences (1e16 neq/cm2 or 1GRad), will be shown.

In addition, future strip readout concepts will be introduced which foresee a digital encoding of the z position and a modified ATLAS strip readout chip (ABC’/ACDC). To minimize the modifications, a lossy fixed-latency priority encoding scheme is employed which can transmit a maximum number of hits per bunch crossing to the ABC’ including an overflow flag bit indicating that individual hits have been lost. Thanks to the facts that digital communication can operate at higher bit rates and that the transmission of a reasonable number of

coincident hits requires much less bits than the number of virtual strips, a very large reduction in the number of wirebonds is achieved. This again helps to lower both production cost and time.

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