The upgrade plans and challenges of the ATLAS first-level trigger towards the HL-LHC

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Motivation for a new trigger

After the Phase-II upgrades to the LHC the luminosity is expected to reach over $5 \cdot 10^{34}$ cm^{-2}s^{-1}. This will push the rate of the single lepton triggers beyond readout capability using the current p_T thresholds. Simply increasing the thresholds is not a viable option since this would mean a loss in physics. The proposed solution is to take tracking information into account already at the hardware based first level (L1) trigger which has been shown to reduce the trigger rates to an acceptable level. Previously this has only been done at the higher software based levels of the ATLAS three tiered trigger scheme. The goal is to have the upgrades installed after the LHC long shutdown 3, beginning in 2022.

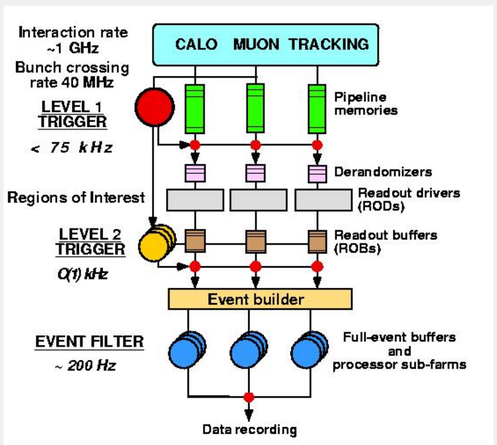


Fig. 1: The current trigger scheme is separated into three levels.

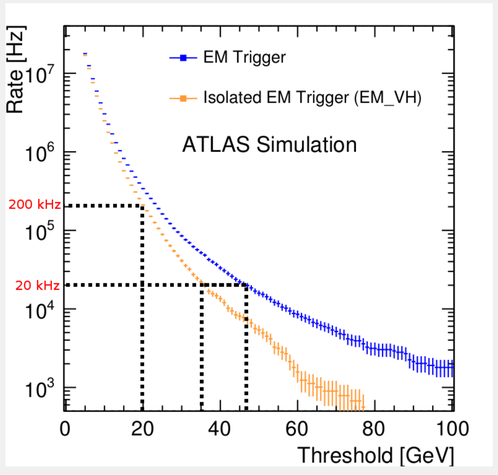
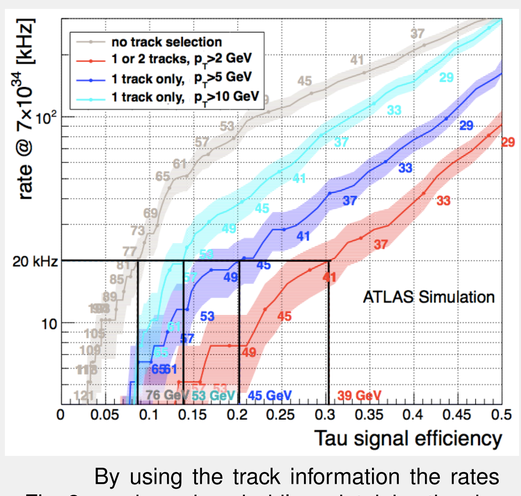


Fig. 2: The p_T thresholds of the single lepton EM trigger would have to be very high in order to maintain a reasonable rate.



By using the track information the rates can be reduced while maintaining the signal efficiency.

A challenging environment

The High-Luminosity LHC (HL-LHC) will increase the number of pile-up events to over 200 primary vertices per bunch crossing. A new all-silicon tracker, the ITK, will be replacing the inner detector to cope with the occupancy and improve the resolution of track parameters. However, the number of tracks per event is too large to perform track reconstruction for the whole detector at the timescale of a L1 trigger. Instead a L0 trigger, similar to the Phase-I L1, can provide so called Regions of Interest (RoI) to the L1 track trigger which then reconstructs the tracks in a subset of the detector.

Split trigger scheme

The L0 trigger will operate at 1 MHz and provide an L0 accept to the L1 trigger with a latency of 6 μs. The L1 will reduce the rate to 400 kHz with another 24 μs latency for a total of 30 μs. The L1 trigger will use the tracking information, full calorimiter granularity and the Muon Drift Tubes (MDT). The MDT can improve the momentum resolution of muons and create sharper turn on curves for the trigger. The place for the MDT in the L0/L1 scheme is uncertain at this point due to the development of the electronics.

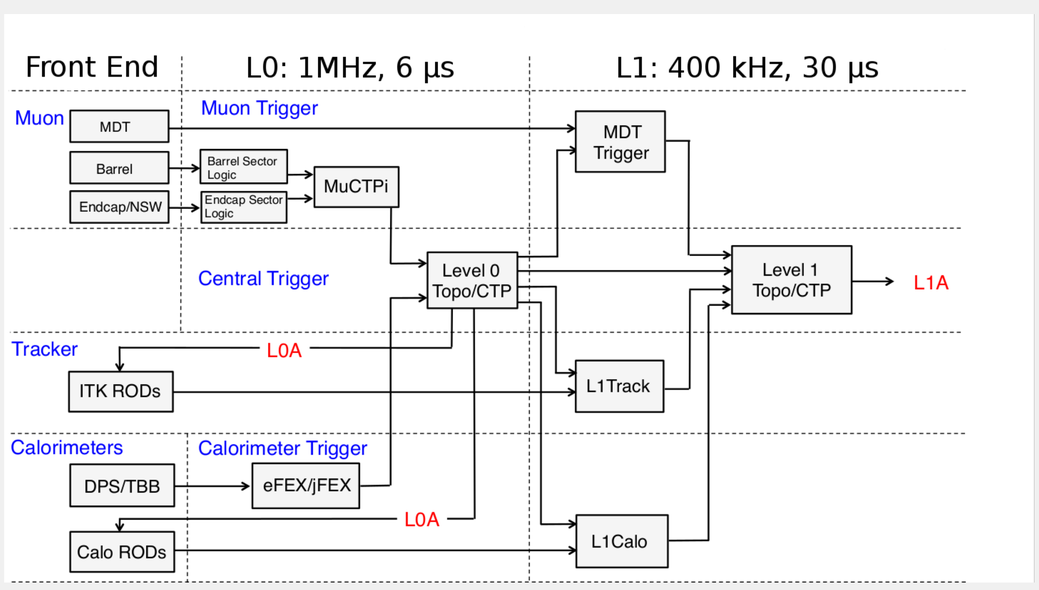


Fig. 4: A graphic of a possible L0/L1 trigger scheme.

Fast readout of tracking information

In order to use the tracking information at L1 the readout of the ITK modules must be fast enough to allow track reconstruction within the total latency. After a L0 accept a Regional Readout Request (R3) is sent to the front-end buffers requesting the data for an RoI. Initial studies showed that 95% of all R3 requests can be readout within the latency when using R3 prioritisation in the Hybrid Chip Controller (HCC) with a 200 kHz L1 accept rate.

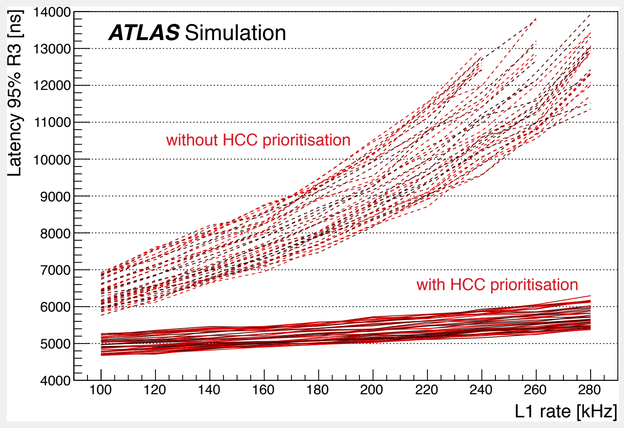


Fig. 5: The simulated readout rates.

With the new baseline of 400 kHz L1 rate, the detector modules with the highest occupancy can not be read out in time using this method and alternative schemes of connections to the HCCs are being investigated.

Parallellized pattern recognition

Chips with ASICs can be used to store precalculated banks of patterns corresponding to tracks above a certain p_T threshold. The chips can process the silicon hit information from the R3 in a parallell fashion to match coarse resolution patterns. Subsequently patterns and the accompanying hits are used to fit the track parameters within the L1 latency budget. Ongoing studies will determine the optimal resolution and number of patterns in a bank in order to achieve sufficient efficiency. A similar project, the Fast Tracker (FTK), is being installed in ATLAS now to provide tracking information to the present high-level trigger.

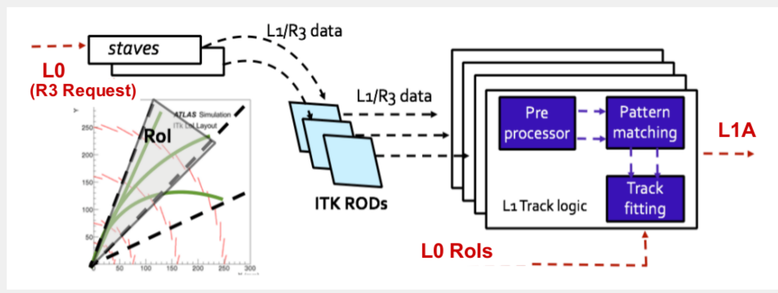


Fig. 6: RoIs can be examined for tracks using pattern matching before applying any fitting algirithms.

Table 1: The mean number of matched patterns (in blue) and size (in red) of pattern banks with more than 99% efficiency. Empty cells are due to bank sizes considered too large for the chips.

Resolution [strips]	5 Layers	8 Layers	10 Layers
32	54, 2.3 M	-	-
64	187, 0.7 M	198, 2.7 M	-
128	537, 0.2 M	669, 0.8 M	255, 1.3 M

Calorimeter trigger

The calorimeter front-end electronics will be replaced and include on-detector digitizers capable of sending the the full granularity information to new back-end electronics and triggers at a rate of 40 MHz. This will improve the energy resolution of the L1 calorimeter trigger and subsequently increase the rejection with sharper E_T cuts and better matching to tracks in a L1 track trigger. The longer latency means that more advanced clustering algorithms can be used to improve the identification of the trigger objects. The trigger can fit in to the L0/L1 scheme by using the Phase-I electron and jet Feature EXtractors (eFEX/jFEX) with a granularity between the current trigger and full resolution.

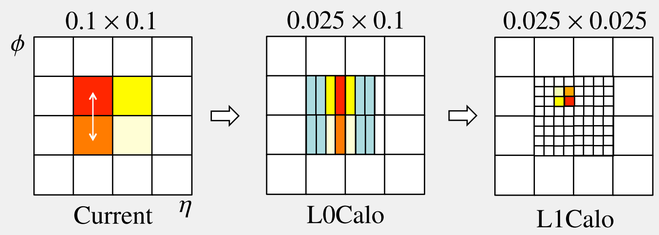


Fig. 7: The higher granularity will give a more precise measurement of the E_T in the L1 calorimeter trigger.

References

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[2] Sutton, M, *Tracking for the ATLAS Level 1 Trigger for the HL-LHC*, CERN, Geneva, ATL-COM-DAQ-2013-085,2013,

[3] De Santo, A, *Towards a Level-1 Tracking Trigger for the ATLAS Experiment*, CERN, Geneva, ATL-COM-DAQ-2014-067, ICHEP2014, 02-09 July 2014

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