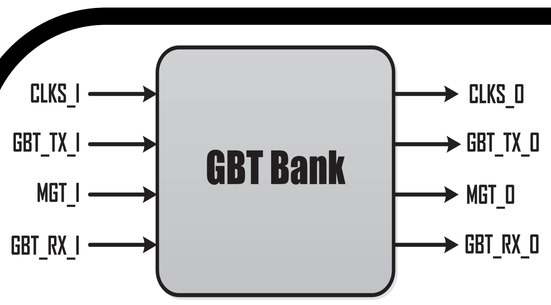


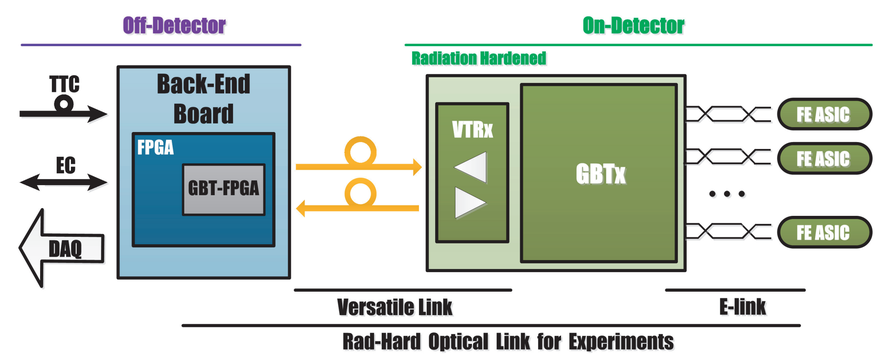
The GBT-FPGA Core *(Features and Challenges)*

YEARS/ANS CERN
PH-ESE-BE

Initiated in 2009 to emulate the GBTx serial link and test the first GBTx prototypes, **the GBT-FPGA project** is now a full library, targeting FPGAs from ALTERA and XILINX, allowing the implementation of one or several GBT links of 2 different types: "Standard" or "Latency-Optimized". These links can be also onfigured to provide any encoding mode offered by the GBTx: the "GBT-Frame", the "8b10b" or the "Wide-Bus". The first major version of this IP Core was released in April 2014 and more than 100 users are members of the GBT-FPGA community. This poster presents the various flavours of the GBT-FPGA kit, and focuses on the challenge of providing a fixed and deterministic latency system both for clock and data recovery for all FPGA families.

The Rad-Hard Optical Link for Experiments

The diagram shown in this section of the poster, depicts a typical system featuring the **"Rad-Hard Optical Link for Experiments"**, highlighting its major components. On the off-detector side, a Back-End (BE) FPGA-based board loading the GBT-FPGA firmware acts as the single-connection point with the detector, transmitting Timing, Triger and Control (TTC) and Experiment Control (EC) data to the Front-End (FE) as well as receiving and forwarding detector data to the central data acquisition (DAQ). On the on-detector side, the GBTx serializer/deserializer (SERDES) ASIC forwards the TTC information to FE ASICs and reads them out through low-speed (80, 160 or 320 Mbps) electrical links named E-links. The physical link between the BE and the GBTx ASIC is known as the "Versatile Link" (VL), a high-speed (4.8 Gbps) optical link which its major component is a custom plug-in module performing optical-to-electrical conversion (and vice versa) named the Versatile Link transceiver (VTRx). It is important to mention that only custom parts are used on-detector since they have to cope with extremely high radiation levels.



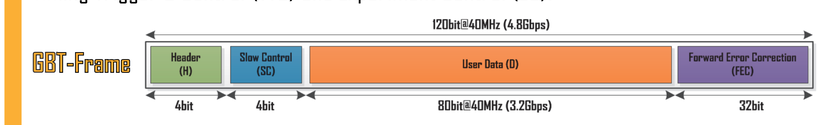
Standard vs Latency-Optimized

Trigger related electronic systems in High Energy Physics (HEP) experiments, such as Timing Trigger and Control (TTC), require a fixed, low and deterministic latency in the transmission of the clock and data to ensure correct event building. On the other hand, other electronic systems that are not time critical, such as Data Acquisition (DAQ), do not need to comply with this requirement. The GBT-FPGA project provides two types of implementation for the transmitter and the receiver: the **"Standard"** version, targeted for non-time critical applications and the **"Latency-Optimized"** version, ensuring a fixed, low and deterministic latency of the clock and data (at the cost of a more complex implementation). With the purpose of providing a graphical comparison of both architectures, the different components that are optimized on the Latency-Optimized version, in order to achieve a fixed, low and deterministic latency are highlighted in green colour in the figure labelled "GBT Bank Diagram".

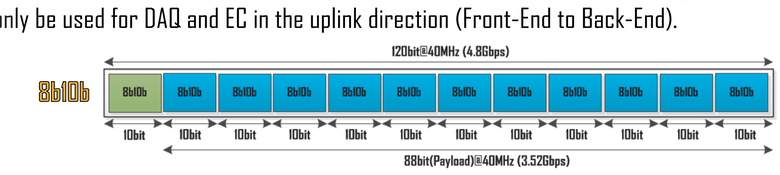
	Standard	Latency-Optimized
Latency	Non Fixed, Higher & Non Deterministic	Fixed, Low & Deterministic
Logic Resources Utilization	Low	Low
Clocking Resources Utilization	Low	High
Clock Domain Crossing	Don't Care	Critical
Implementation	Simpler	Complex

Data frame & Encodings

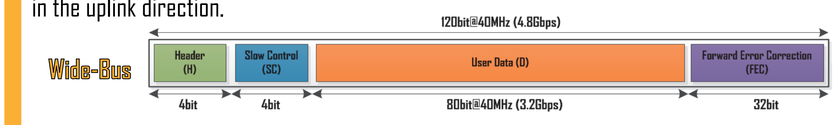
The GBT-FPGA supports the three available encoding schemes proposed by the GBTx:
The**"GBT-Frame"**adopts the Reed-Solomon that can correct bursts of bit errors caused by Single Event Upsets (SEU). This encoding scheme can be used for Data Acquisition (DAQ), Timing Trigger & Control (TTC) and Experiment Control (EC).



The **"8b10b"**provides 4bit more than the GBT-Frame to be used by the user at the cost of no error correction and limited error detection capability. This encoding scheme can only be used for DAQ and EC in the uplink direction (Front-End to Back-End).



For the **"Wide-Bus"**, the FEC field is fully replaced by user data at the cost of no error detection nor correction capability. This encoding scheme can only be used for DAQ and EC in the uplink direction.



Status

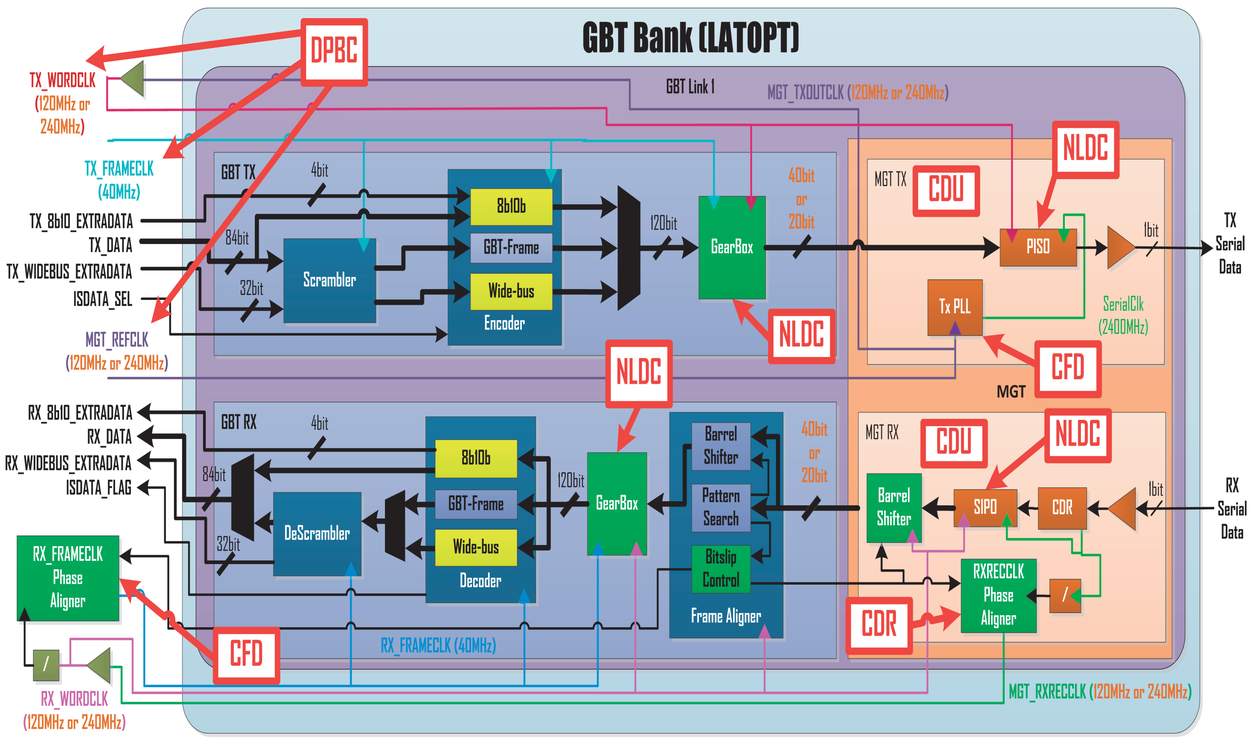
- **GBT-FPGA Development Kit Includes:**
  - HDL Sources
  - Example Designs
  - Documentation
  - Video Tutorials
  - TCL Scripts
- **Available For:**
  - Xilinx Virtex 6 (GLIB, ML605)
  - Xilinx Kintex 7 (FC7, KC705)
  - Xilinx Virtex 7 (VC707)
  - Altera Cyclone V (SAT, Cyclone V GT Devkit)
  - Altera Stratix V (AMC40)
- **Encodings & Optimizations:**
  - Encodings: GBT-Frame, Wide-Bus, 8b10b
  - Optimizations: Standard, Latency-Optimized
- **To Do:**
  - Integrate New Versions (Arria 10, Igloo2, ...)
  - Different Studies (More Measurements, etc.)
  - Get Feedback From Users :-)

Potential Uncertainty Points in the Latency-Optimized Version

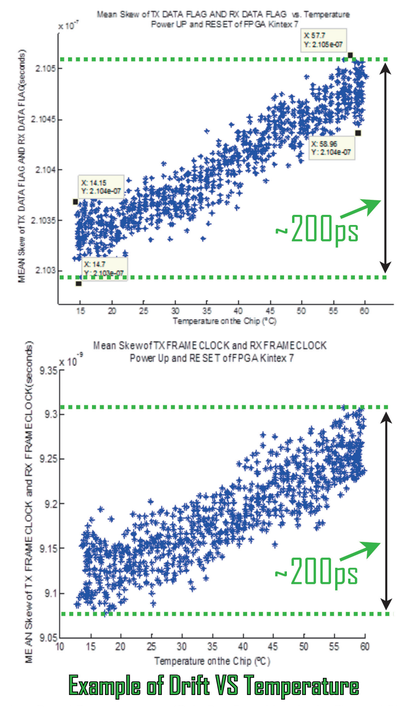
Achieving fixed and deterministic phase in clocks as well as low, fixed and deterministic latency in data transmission/reception when implementing the **Latency-Optimized** version of the GBT-FPGA core requires identifying and properly managing the different **Potential Uncertainty Points (PUPs)** of the GBT-FPGA core-based system. Since these uncertainty points are implementation and configuration dependent, dealing with systems featuring the Latency-Optimized version of the GBT-FPGA core may become very challenging, especially in multi-GBT Link configurations.

The different PUPs within the GBT Bank have been already properly managed, being only necessary to constraint some critical paths of the GBT Link(s) during in-system implementation. On the other hand, the external PUPs have to be managed by the user (although the GBT-FPGA project provides example designs including custom modules for this purpose).

The block diagram on the right of this text depicts a GBT Bank featuring one GBT Link, highlighting the internal and external PUPs.



Measurements

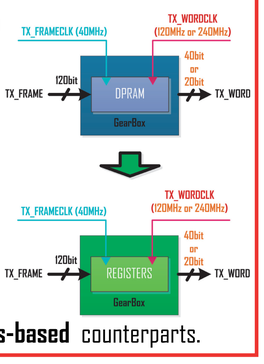


Example of Drift VS Temperature

Board-to-Board Communication (Only One Board Inside the Thermal Chamber)

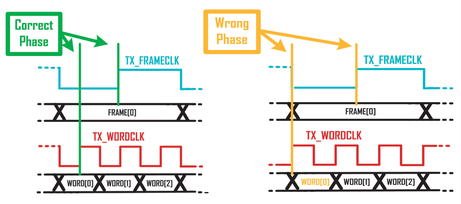
Non Latency Deterministic Components (NLDC)

Certain components, such as FIFOs or DPRAMs used for Clock Domain Crossing, may lead to uncertainty and undesired extra cycles in the latency of the data path. For this reason, in the Latency-Optimized version, these components are replaced by **registers-based** counterparts.



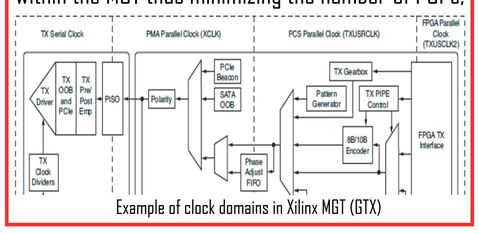
Deterministic Phase Between Clocks (DPBC)

Due to the register-based Clock Domain Crossing approach used in the Latency-Optimized version, the phase of the different clocks used by the GBT Bank must be carefully controlled to **ensure fixed delay** and **avoid metastability**.



MGT Clock Domain Unification (CDU)

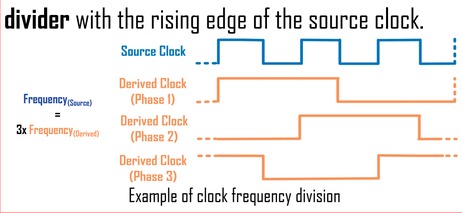
The frequency of the clocks and the width of the data buses in the MGT of the GBT Link were selected with the aim of **reducing as much as possible the number of different clock domains** within the MGT thus minimizing the number of PUPs,



Example of clock domains in Xilinx MGT (GTX)

Clock Frequency Division (CFD)

When dividing the frequency of a clock, the rising edge of the derived clock may lock onto any of the rising edges of the source clock. In order to avoid this uncertainty in the phase of the derived clock, is necessary to **synchronize the reset of the clock divider** with the rising edge of the source clock.



Example of clock frequency division

Clock & Data Recovery (CDR)

In the MGT RX of the GBT Link, during the clock and data recovery from the incoming data stream, the frequency of the serial clock is divided by a certain factor N. Due to the utilisation of Dual Data Rate (DDR) by the CDR, **the recovered clock may lock onto any of both (rising and falling) edges of the serial clock**. This gives 2xN possible phases for the recovered clock and also, the same number of possible bitslips in the recovered data. This clock and data uncertainty issue is worked out by using a custom monitor logic embedded into the GBT Link.

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Web site: https://espace.cern.ch/GBT-Project/GBT-FPGA/default.aspx
SVN repository: https://svn.cern.ch/reps/ph-ese/be/gbt_fpga

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