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The GBT-FPGA Core: Features and Challenges

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Initiated in 2009 to emulate the GBTx serial link and test the first GBTx prototypes, the GBT-FPGA project is now a full library, targeting FPGAs from ALTERA and XILINX, allowing the implementation of one or several GBT links of 2 different types: "Standard"or "Latency-Optimized". The first major version of this IP Core was released in April 2014. This paper presents the various flavours of the GBT-FPGA kit, and focuses on the challenge of providing a fixed and deterministic latency system both for clock and data recovery for all FPGA families.

Summary

Initiated in 2009 to emulate the GBTx serial link in Stratix II and Virtex 5 FPGAs and test the first GBTx prototypes, the GBT-FPGA project developed first to provide the users with a basic "starter kit"allowing them to get used to the GBTx protocol. As the features of the GBTx ASIC inflated during design phase together with the users'requirements, the GBT-FPGA project naturally followed and grew up as well. This GBT-FPGA core is now a full library, and its first major version was released in April 2014 and more than 100 users are members of the GBT-FPGA community. This very versatile IP Core is currently targeting FPGAs from ALTERA (Cyclone V, Stratix V) and XILINX (Virtex 6, Virtex 7, Kintex 7) as well as many reference designs, allowing the implementation of one or several GBT links of 2 different types: "Standard"or "Latency-Optimized"(providing low, fixed and deterministic latency either on Tx, Rx or on both). These links can be also configured to provide any encoding mode offered by the GBTx: the "GBT-Frame"mode (Reed-Solomon based), the "8b10b"mode or the "Wide-Bus"mode (no encoding). The GBT-FPGA core is freely available from SVN, and can be instantiated on Back-End FPGAs, but it can also be used as a GBTx emulator for the serial link. The GBT-FPGA core (in its Cyclone V Latency-optimized version) was intensively used to perform qualification, characterization and extensive radiation tests on the GBTx ASIC.
This paper presents the various flavours of the GBT-FPGA kit, and focuses on the challenge of providing a fixed and deterministic latency system both for clock and data recovery for all FPGA families.

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