Contribution ID: **18** Type: **Poster**

Applications of Cascaded Phase Lock Loop (PLL) Blocks inside Field Programmable Gate Array (FPGA)

Tuesday 23 September 2014 17:09 (1 minute)

Signals with various timing relations can be generated inside FPGA conveniently with internal phase lock loop
(PLL) blocks. When multiple PLL blocks are cascaded together. In this paper, clocks
generated by cascaded PLL with slightly difference in frequencies are studied. They are used to produce pulse pairs with precise timing delay control at 0.98 ps/step. They are also used to generate calibration signals inside FPGA based TDC with evenly spread timing spectrum. The cascaded PLL can also be used for relative phase measurement of several input clocks. The firmware of the FPGA and the measurement results are presented.

Summary

unfinished.
To be added

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Session Classification: First Poster Session

Track Classification: Logic