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Architecture of the Upgraded BCM1F Backend Electronics for Beam Conditions and Luminosity Measurement - Hardware and Firmware

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The Beam Radiation Instrumentation and Luminosity Project of the CMS experiment, consists of several beam monitoring systems. One system, the upgraded Fast Beams Condition Monitor, is based on 24 single crystal CVD diamonds with a double-pad sensor metallization and a custom designed readout. Signals for real time monitoring are transmitted to the counting room, where they are received and processed by new back-end electronics designed to extract information on LHC collision, beam induced background and activation products. Data in the form of histograms is transmitted to the DAQ. The system architecture and signal processing algorithms will be presented.

Summary

The Fast Beam Conditions Monitor (BCM1F) detector is a part of the CMS Beam Radiation Instrumentation and Luminosity Project (BRIL). The increased performance expected of the LHC with energy of up to 14 TeV, higher luminosity and 25 ns bunch spacing is a challenge for the detector systems and increase the importance of real-time beam monitoring at high rates. The BCM1F is designed to monitor the flux and timing of particles originating from the proton-proton interactions and machine-induced-background (MIB) particles using 24 single crystal CVD diamond sensors positioned at a distance of ±1.8 m from the interaction point. Signals from the detectors are shaped and amplified by a front-end pre-amplifier ASIC and transmitted through optical fibers.

The BCM1F back-end electronics is designed to receive signals from the detector via 48 optical channels. The architecture of the system is based on MicroTCA technology. It assumes using 12 AMC cards with a single FMC connector for receiving signals from the detector, 2 AMCs for measurement of the Beam Pick-up Timing for Experiments (BPTX) signals and 2 AMCs for the slow control of the front-end electronics. For signals digitizing 12 FMC mezzanines with 4 channels, 8 bit ADCs at a sampling rate 1.25 GS/s are considered to be used. The mezzanines configured in 1 channel operating mode at 5 GS/s sampling rate can be used for the BPTX signals measurement. The slow control module will use 2 FMC mezzanines with 8 SFP/SFP+ cages.

The firmware design must be capable of processing signals at very high input rates (270 MHz) without introducing any dead time. It will provide information about collisions, MIB and activation products. Samples will be processed in FPGAs on AMC carrier boards, put into histograms and sent to the BRIL data acquisition system. The data processing algorithm is being designed to be able to recognize signal peaks from the detector with a minimum time resolution of ˜12 ns, which corresponds to the maximum overlap of two pulses that can be recognized as separate from the ASIC. The single pulse FWHM is 10 ns. Various methods of the amplitude and time measurement are being tested. Information about a peak occurrence will be stored in histograms: total number of counts in time, and in amplitude. Additionally one orbit of RAW data is possible to be collected every Lumi Nibble (2ˆ12 orbits) and sent to the DAQ, for efficiency studies. The data storage will consume most of the FPGA memory resources (up to 85%) that hence the more complex algorithms can be used only for offline analysis.
The structure of the system, data flow and considered algorithms will be presented along with the current status of the readout system development.

Author: ZAGOZDZINSKA, Agnieszka Anna (Warsaw University of Technology (PL))

Presenter: ZAGOZDZINSKA, Agnieszka Anna (Warsaw University of Technology (PL))

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