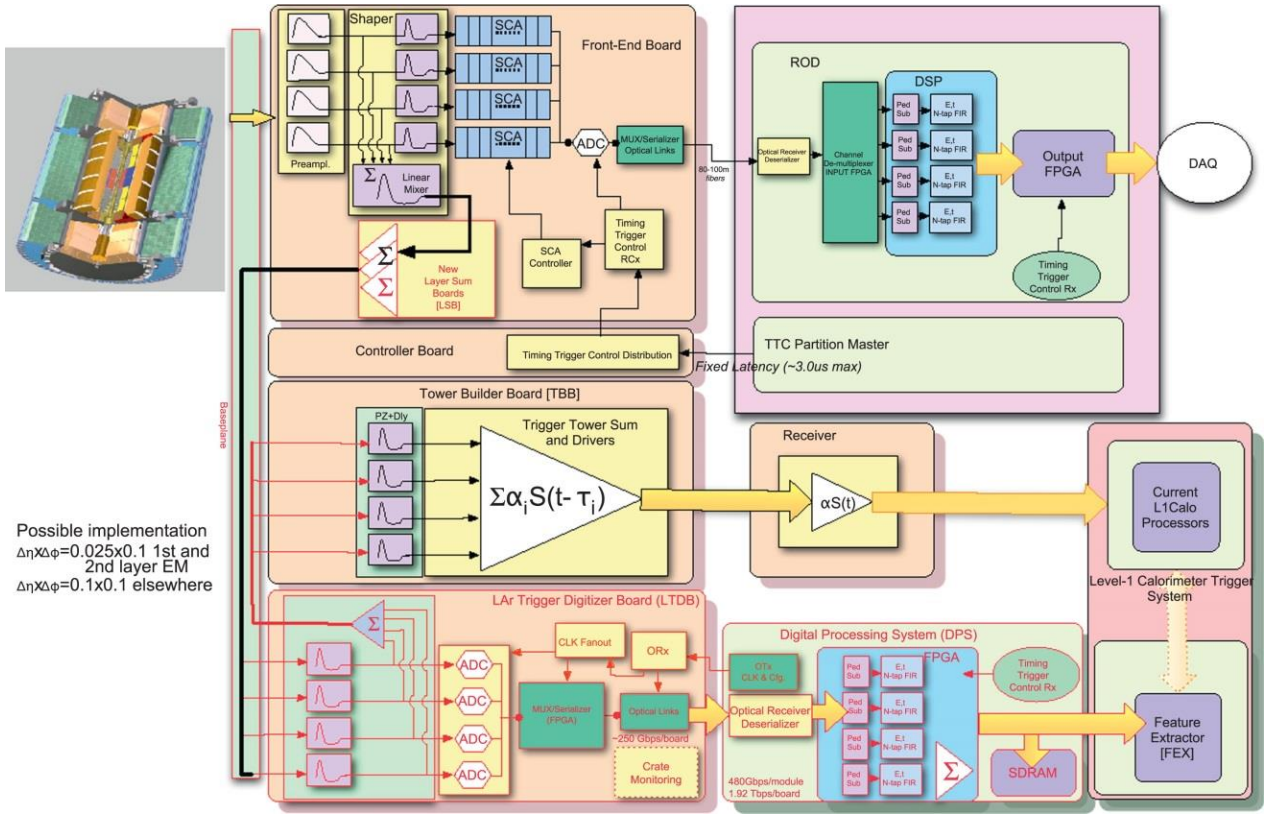
8-Gbps-per-channel radiation-tolerant VCSEL drivers for the LAr Readout upgrade

Xiaoting Li, Futian Liang, Datao Gong
Southern Methodist University
TWEPP 2014

Outline

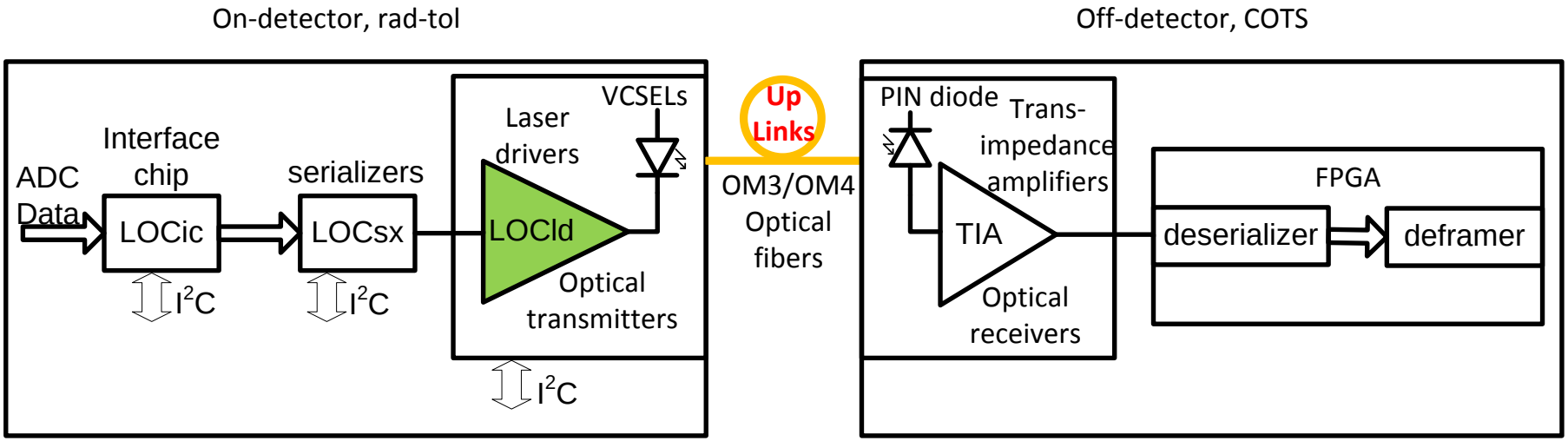
- Introduction
- Design of 8-Gbps VCSEL driver LOCld1
- Test of LOCld1
- Two-channel VCSEL driver LOCld2
- Summary

ATLAS LAr Calorimeter Phase-I front-end readout upgrade



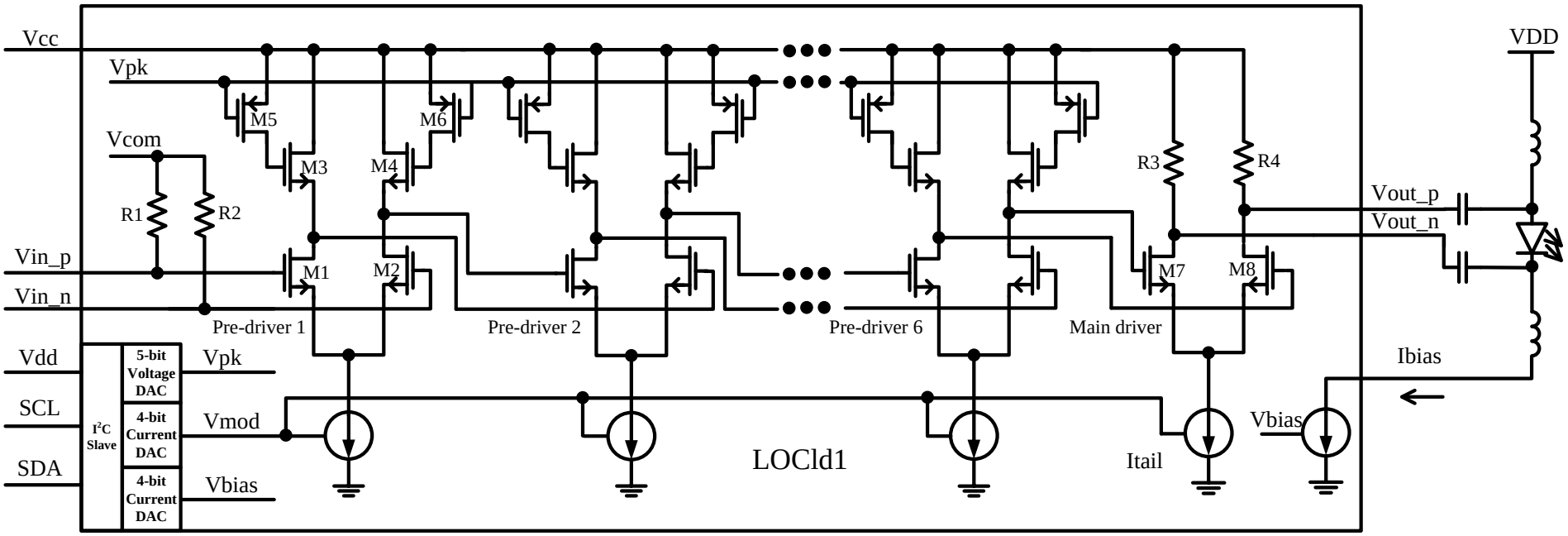
- LAr Trigger Digitizer Boards (LTDB) will be installed in 2018 (Phase-I upgrade)
- Consecutive trigger digital data readout requires about 250 Gbps/board
- LOCld1 and LOCld2 are designed for ATLAS LAr readout optical link

Optical link for new LTDB



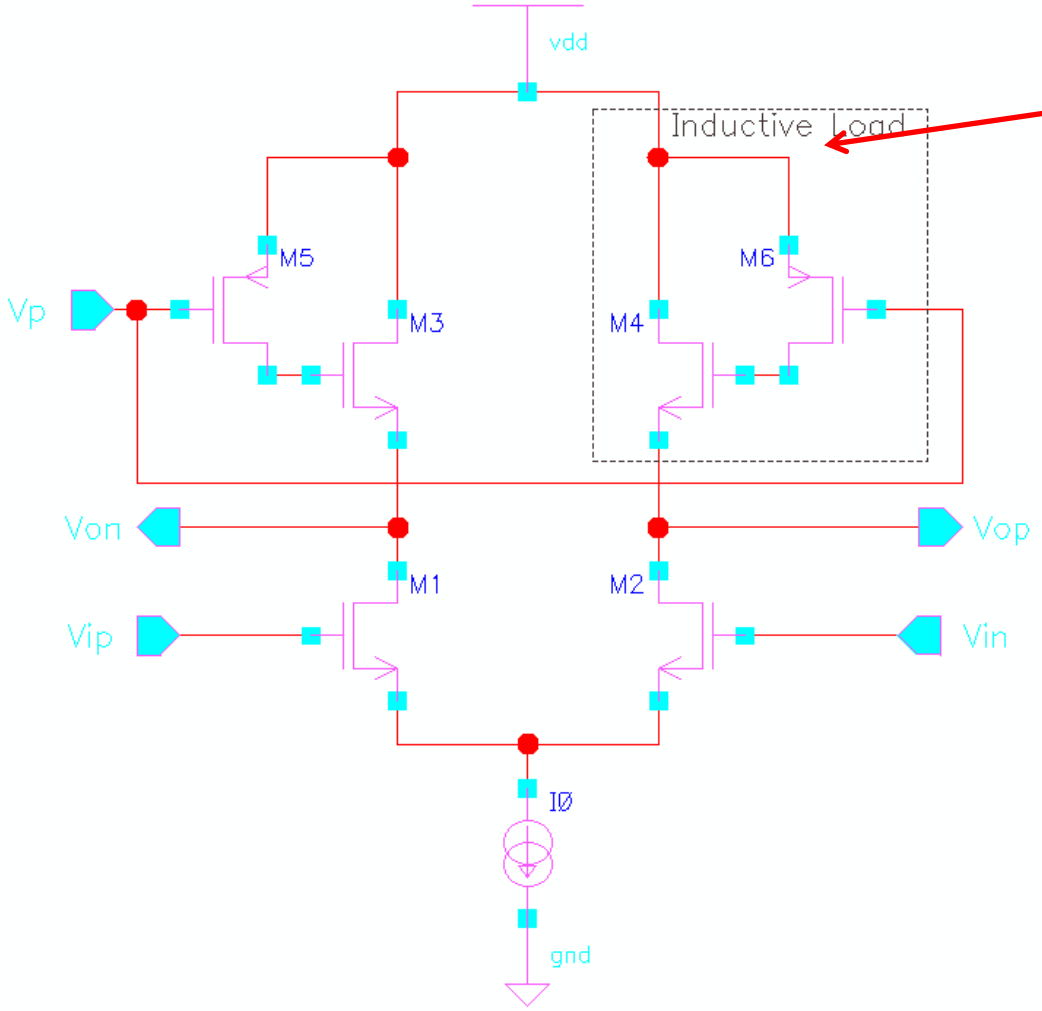
- Requirements: **low power**, **radiation tolerance**, **high bandwidth,** 6~8 mA modulation current(typical VCSEL driver)
- Based on a commercial 0.25 µm Silicon-on-Sapphire CMOS technology, the design goal is **8 Gbps**.
- Fabricated the first version, LOCld1, in 2012; The second version added I2C salve controller in 2013; The two-channel version, LOCld2, fabricated in 2013.
- Built a low-footprint dual-channel optical transmitter module (MTx)

Differential Amplifiers design



- 6 stage differential amplifier with active shunt-peaking, 3.3V power supply
- peaking strength programmable for radiation effect
- I2C slave integrated, thanks CERN ME group for sharing HDL code
- VCSEL modulation current and biasing current are programmable

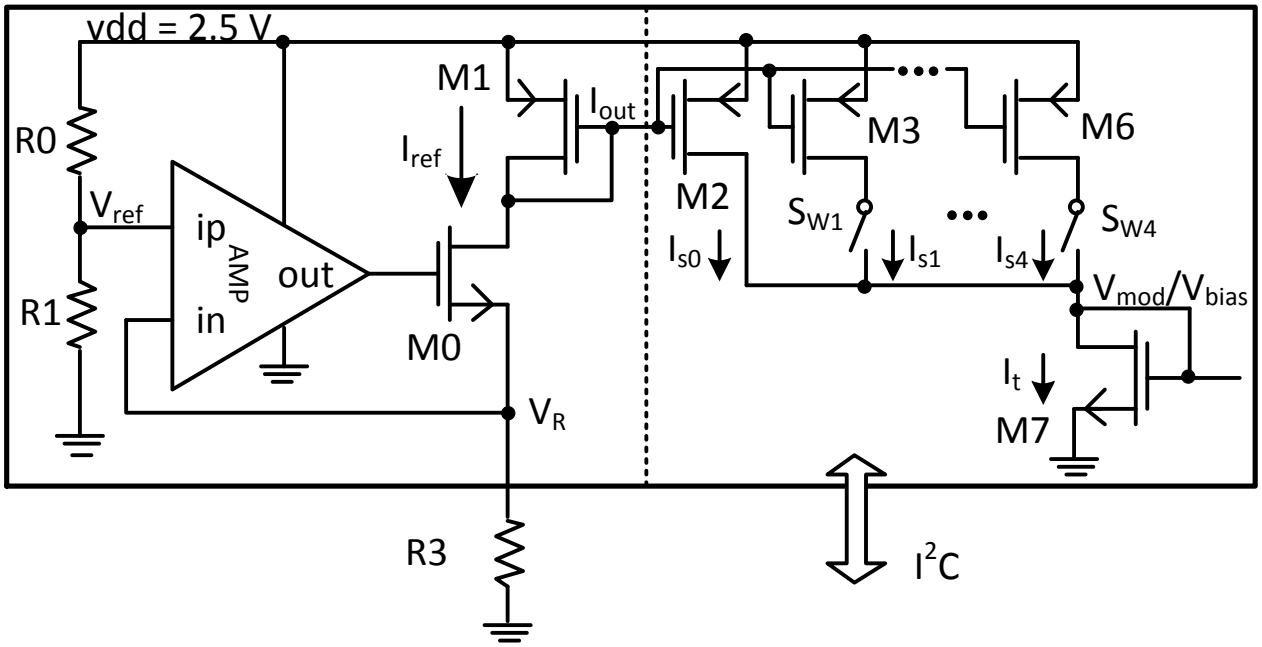
Active Shunt Peaking



$$\frac{1}{g_m}\left[\frac{1+sC_{GS}R_G}{1+sC_{GS}/g_m}\right]$$

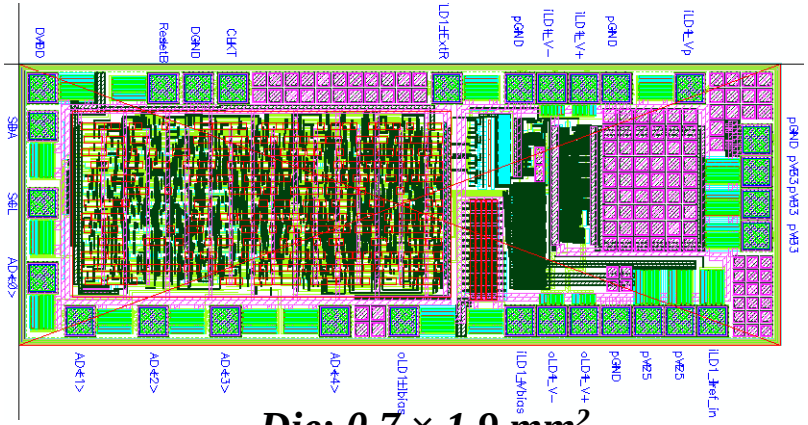
- Active shunt peaking, inductive load region between the zero (low) and pole (high).
- PMOS M6 is equivalent to a resistor (R_G), peaking strength programmable
- Full transistors design, small area.

Current source regulator

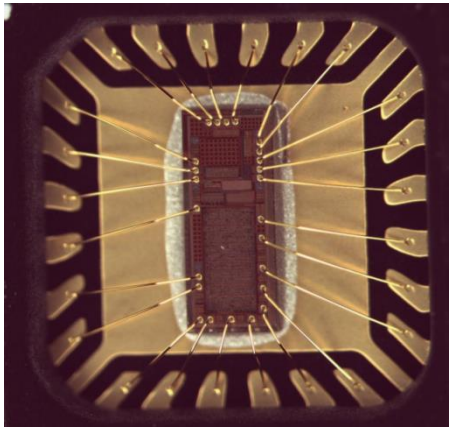


- Observed biasing current change in first version due to V_{th} shift
- Simple100 µA constant current source as the reference, not sensitive to V_{th} shift
- An off-chip resistor R3 is needed.

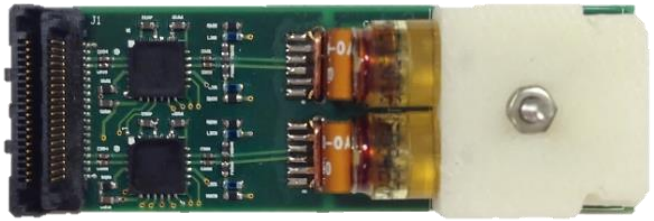
LOCld1 packaged for Test



Die: 0.7 × 1.9 mm^2



24-pin QFN 4x4mm

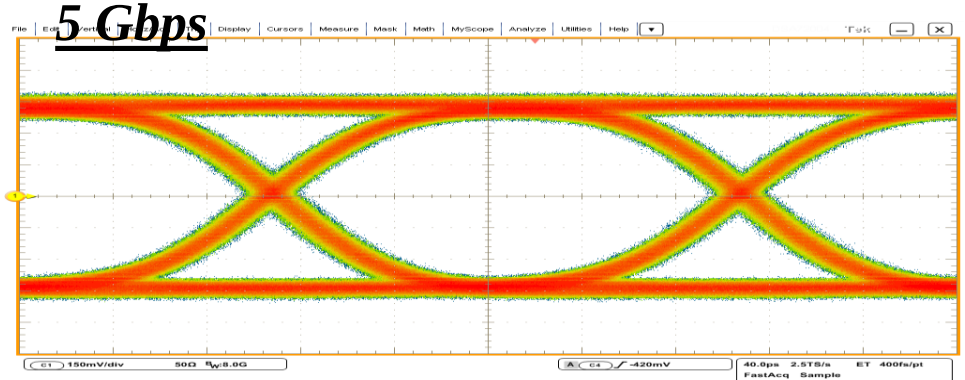


MTx Module W:L:H 15:45:6mm

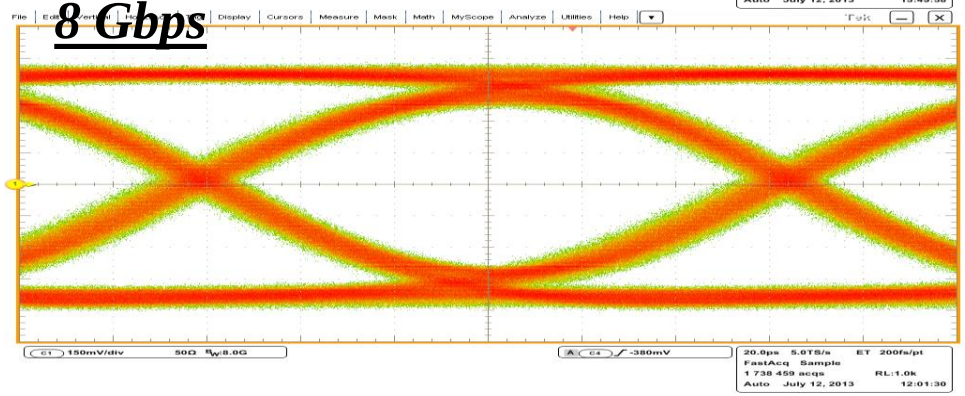
MTx with Carrier board

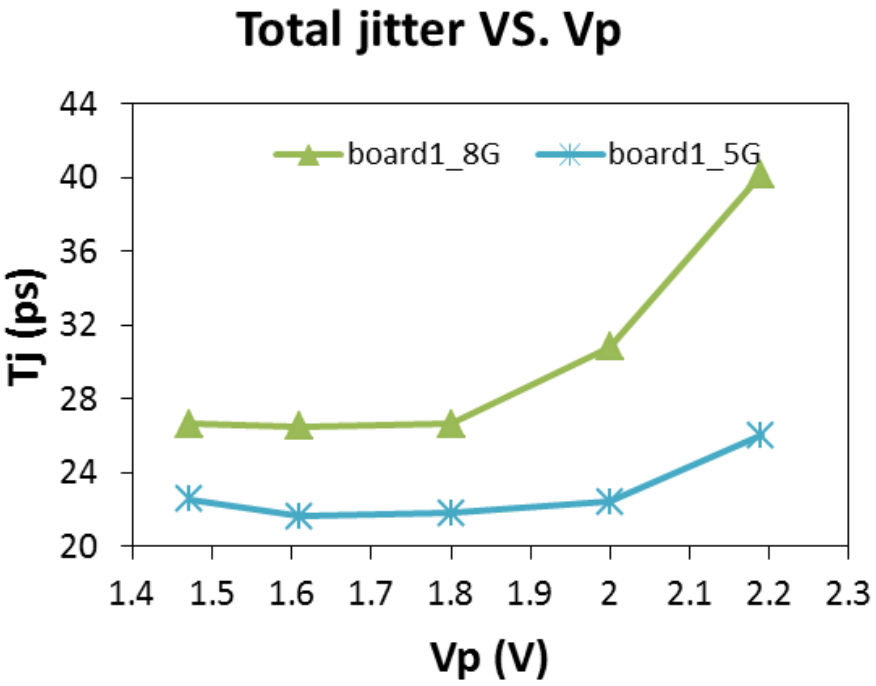
LOCld1 electrical signal Jitter

5 Gbps



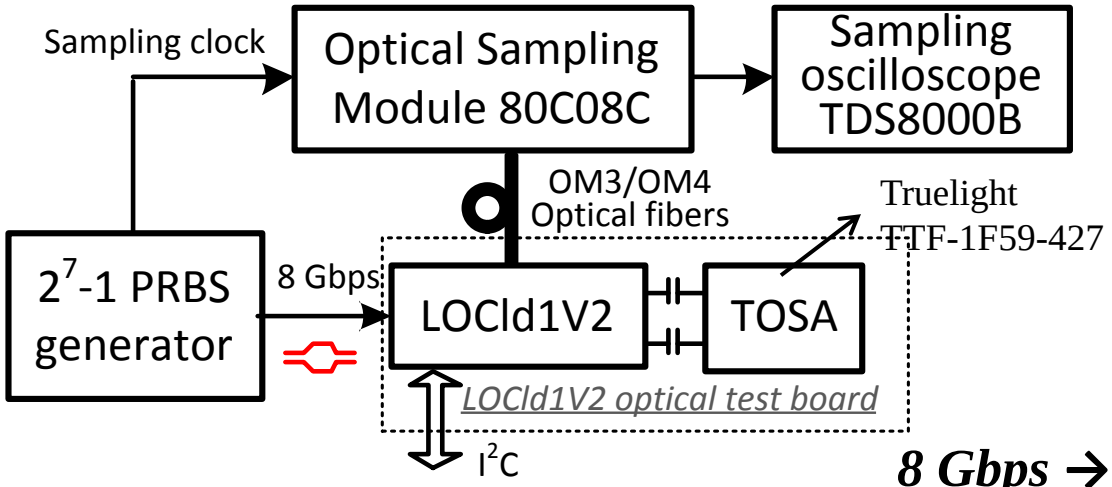
8 Gbps



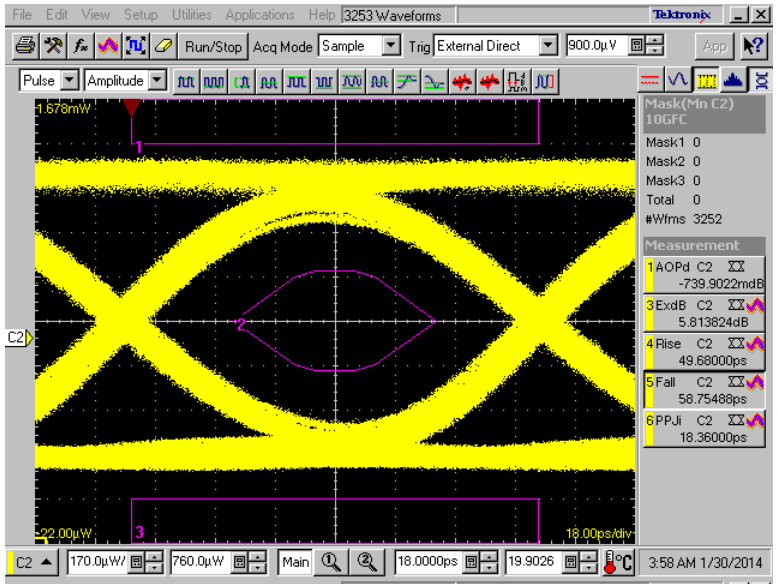


- Measure the electronic signal jitter with 200 mV differential PRBS signal input
- Active shunt peaking improves jitter of 8 Gbps signal transmission but not help much for 5 Gbps
- The programmable peaking strength is useful to tolerant V_{th} shift.

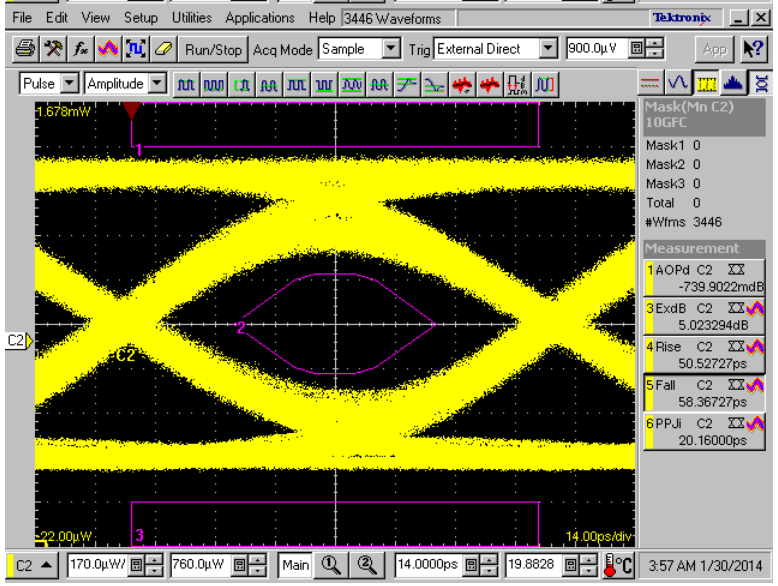
Optical eye diagram



8 Gbps →



10 Gbps →



Test Settings:

Vp = 2.25 V

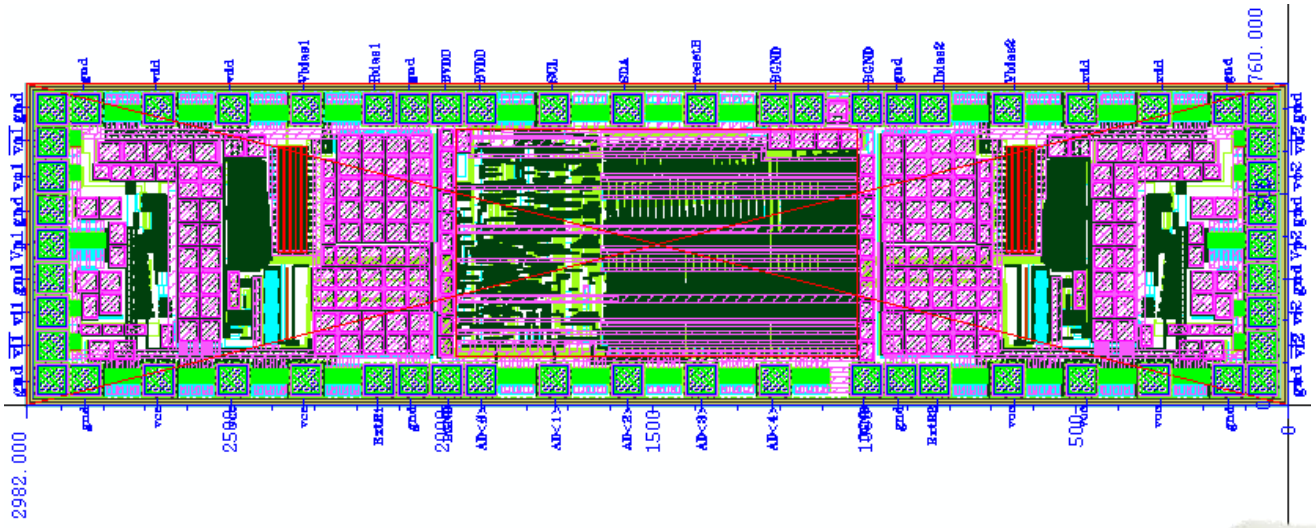
Ibias = 6 mA

Imod = 6.4 mA

Input diff: 200mV

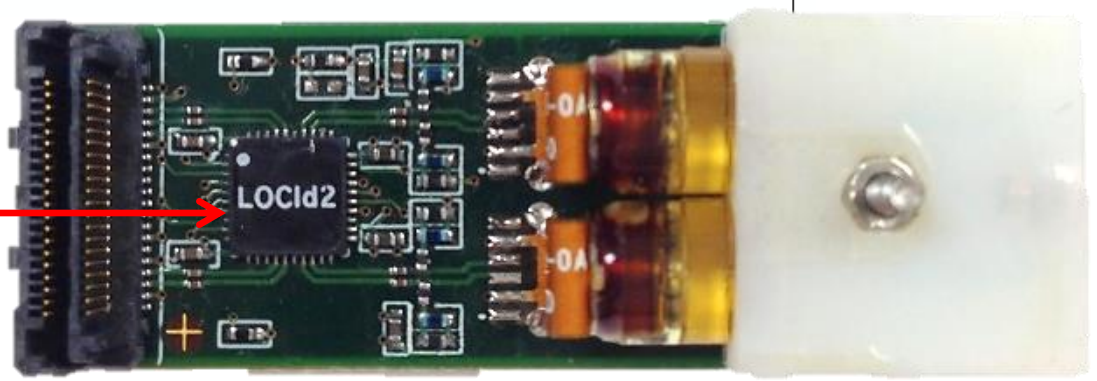
Measured Power: 200mW

LOCld2



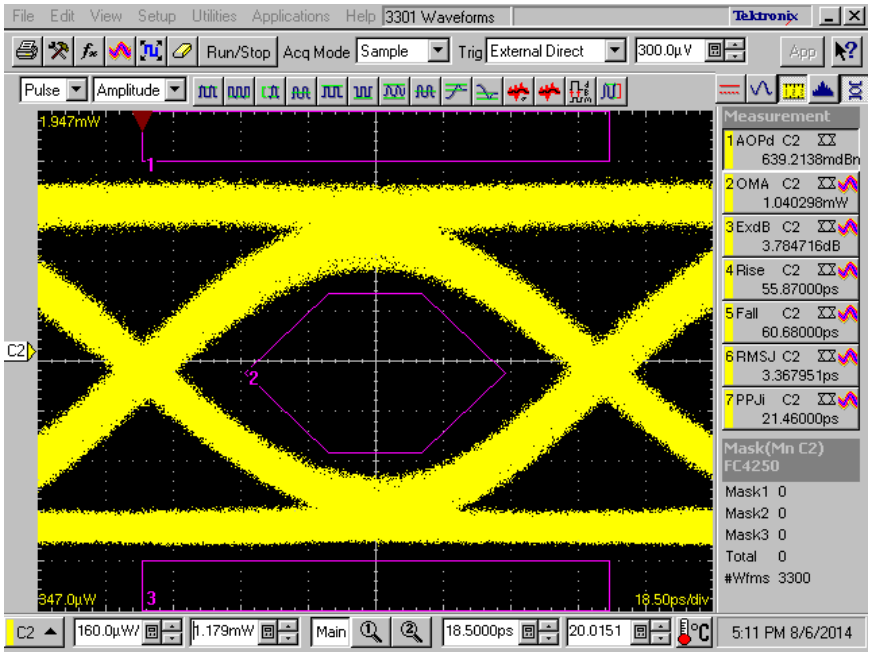
Die size:
0.76 × 2.982 mm²

40-pin QFN
5x5 mm²

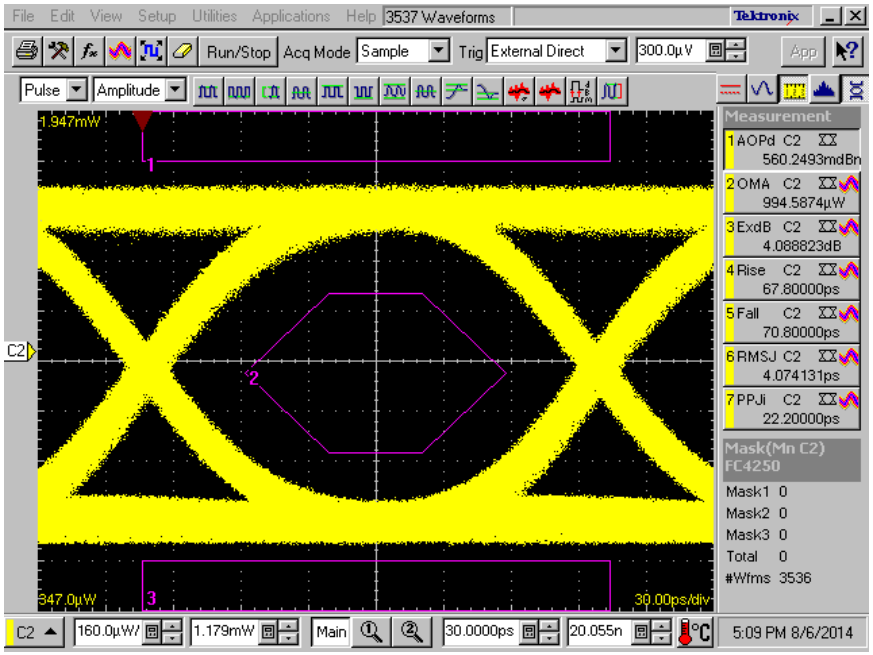


- LOCld2 include two channel drivers on one die, share I2C controller etc.
- Save package and PCB cost in assembling

LOCld2 lab tests



8 Gbps



5 Gbps

- Very preliminary, incomplete test at lab so far
- Settings: Vp = 2.25 V, Ibias = 8 mA, Imod = 8 mA, TOSA: Truelight TTF-1F59-427
- Similar performance as LOCld1: Total jitter (pk-pk) is about 25 ps, no more than 30 ps at 8 Gbps.

Summary

- Design and fabricated VCSEL laser driver, LOCld1 and LOCld2, for ATLAS LAr readout Phase-I upgrade
- Both chips are assembled into a customized small factor optical module, MTx.
- Both chips achieve design goal, work above 8 Gbps, consuming 200 mW per channel.