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8-Gbps-per-channel Radiation-tolerant VCSEL Drivers for the LHC Detector Upgrade

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We present the designs and testing results of a single-channel and a two-channel VCSEL driver and a four-channel array VCSEL driver ASICs for the LHC detector upgrade. All ASICs are fabricated in a commercial 0.25-μm Silicon-on-Sapphire CMOS technology. LOCld1 and LOCld2 are designed to drive differentially VCSEL TOSAs, whereas LOCld4 is designed to drive a VCSEL array die. LOCld1/LOCld2 and LOCld4 pass the 10-Gbps and 8-Gbps eye masks, respectively. The radiation tolerance of LOCld1 has been qualified with x-ray and neutron beam test.

Summary

We have designed three 8-Gbps-per-channel VCSEL driver ASICs for LHC detector upgrade, including a single-channel driver LOCld1, a two-channel driver (LOCld2), and a four-channel array VCSEL driver (LOCld4). All ASICs are fabricated in a commercial 0.25-μm Silicon-on-Sapphire CMOS technology. LOCld1 and LOCld2 are designed to drive differentially VCSEL TOSAs, whereas LOCld4 is designed to drive a VCSEL array die.

LOCld1 consists of 7 stages of differential amplifiers, a 5-bit voltage DAC, two 4-bit current DACs, and an I2C slave controller. LOCld2 ASIC encloses two identical VCSEL drivers sharing one I2C slave controller. The VCSEL array driver LOCld4 has four channels. Each channel consists of six pre-driving stages and one main-driving stage that with an open-drain output structure. We separate the power supplies for the pre-drivers and the main driver as Vpre and Vvcsel. The Vpre of four channels is shared in the die, while the Vvcsel is separated inside and can be connected together outside the die. All ASICs use an active inductor shunt-peaking technique with programmable strength to extend the bandwidth. To immune from the single event upsets (SEUs), internal registers of I2C slave module are protected with Triple Modular Redundancy (TMR). Our analysis shows that the modulation current, the bias current and the peaking strength to decrease during irradiation. To solve the problem we use a current source that is insensitive to transistor threshold voltage shift as the reference of the modulation current and the bias current and an integrated voltage DAC to program the active peaking strength via an I2C interface.

LOCld1 and LOCld2 have been packaged in quad-flat no-leads (QFN) packages and tested. Both ASICs achieved reliable operation at the target 8-Gbps data rate (also worked well at 10 Gbps). The measured total jitter is less than 19 and 21 ps (peak-peak at the bit error rate (BER) of 1×10-12) at 8 and 10 Gbps data-rates, respectively. The BER is less than 1×10-12 at the 95% confidence level. The power consumption is about 200 mW per channel. LOCld4 has been assembled in a custom-made array optical transmitter module. Each channel of LOCld4 passed the 8-Gbps eye mask. The radiation tolerance of the ASICs has been tested and the detailed test results will be presented in the conference.

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