Contribution ID: **159** Type: **Poster**

SAMPA Chip: a New ASIC for the ALICE TPC and MCH Upgrades

We will present the technical details of a new 130 nm CMOS ASIC, aimed to replace the present front-end electronics of two detectors (TPC and MCH) of the ALICE-LHC experiment. The SAMPA ASIC is an evolution of the presently used TPC front-end electronics in several ways. The SAMPA ASIC will provide of 32 channels either negative or positive polarity operation, 2 peaking time and 3 sensitivity configuration, continuous or triggered read-out and data serialization at 320Mbps. Chip performance, both from simulations and from first tests of the first prototype will be presented and discussed.

Summary

In order to operate the ALICE-TPC (Time Projection Chamber) at a PbPb collision rate of 50kHz, several limitations imposed by the current operation of the detector need to be overcome. The present MWPC based read-out chambers will be replaced by GEM detectors, which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As the drift time will be higher than the average time between interactions, a trigger-less continuous read-out is implemented. This implies the upgrade of the existing front-end electronics with a new read-out ASIC, the SAMPA ASIC, providing continuous read-out. Furthermore, in order to operate the muon chambers (MCH) with an interaction rate of 50kHz the present front-end electronics cannot be used and will be replaced by the SAMPA ASIC as well. The SAMPA ASIC adapts to different detector signals with programmable parameters.

The SAMPA ASIC is an evolution of the presently used TPC front-end electronics, where front-end amplifier and shapers sit in the 16-channel PASA ASIC. The 16-channel ALTRO chip digitizes, processes, compresses and stores the data in a multi-event memory. The SAMPA ASIC will integrate 32 channels per chip of the full data processing chain and support continuous and triggered read-out. SAMPA contains positive/negative polarity Charge Sensitive Amplifiers (CSA), which transform the charge signal into a differential semi-Gaussian voltage signal, that is digitized by a 10-bit 10 Msamples/s ADC. After the ADC, a digital signal processor eliminates signal perturbations, distortion of the pulse shape, offset and signal variation due to environmental and/or run condition variations. The data read-out takes place continuously at a speed of up to 1.28 Gbps via four 320 Mb/s e-links. The data read-out can be performed in continuous mode or triggered mode. In continuous mode, for each ch, independently, the read-out of a programmable number of samples is performed trigger-less if the input signal exceeds the programmable threshold value.

The CSA shaping time can be configured to values of 80 ns and 160 ns for the TPC and 300 ns for the MCH. The sensitivity can be set to 20 or 30 mV/fC for the TPC and 4 mV/fC for the MCH by two external pins. The maximum amplitude of the output pulse is 2 Vpp. The power consumption of the analog front-end is 7mW per channel with ENC specification of 540e for 160ns of peaking time, 30mV/fC of sensitivity and linearity lower than 1%. The cross-talk specification is lower than 0.3% for 18.5pF of detector capacitance.

The chip is being designed in 130 nm CMOS technology with nominal voltage supply of 1.2 V and a first test prototype was submitted to fabrication.
The simulation results, as well as the first result of the tests the prototype will be presented an discussed.

Primary author: HERNANDEZ HERRERA, HUGO DANIEL (Polytechnic School of the University of São

Paulo)

Co-authors: CAVALCANTE DE SOUZA SANCHES, Bruno (Universidade de Sao Paulo (BR)); GUZZO NEVES, Heitor (Universidade de Sao Paulo (BR)); GAMEIRO MUNHOZ, Marcelo (Universidade de Sao Paulo (BR)); Dr BREGANT, Marco (Universidade de Sao Paulo (BR)); Dr VAN NOIJE, Wilhelmus (Universidade de Sao Paulo (BR))

Presenter: HERNANDEZ HERRERA, HUGO DANIEL (Polytechnic School of the University of São Paulo)

Track Classification: ASICs