# SET Detection and Compensation and Its Application in PLL Design

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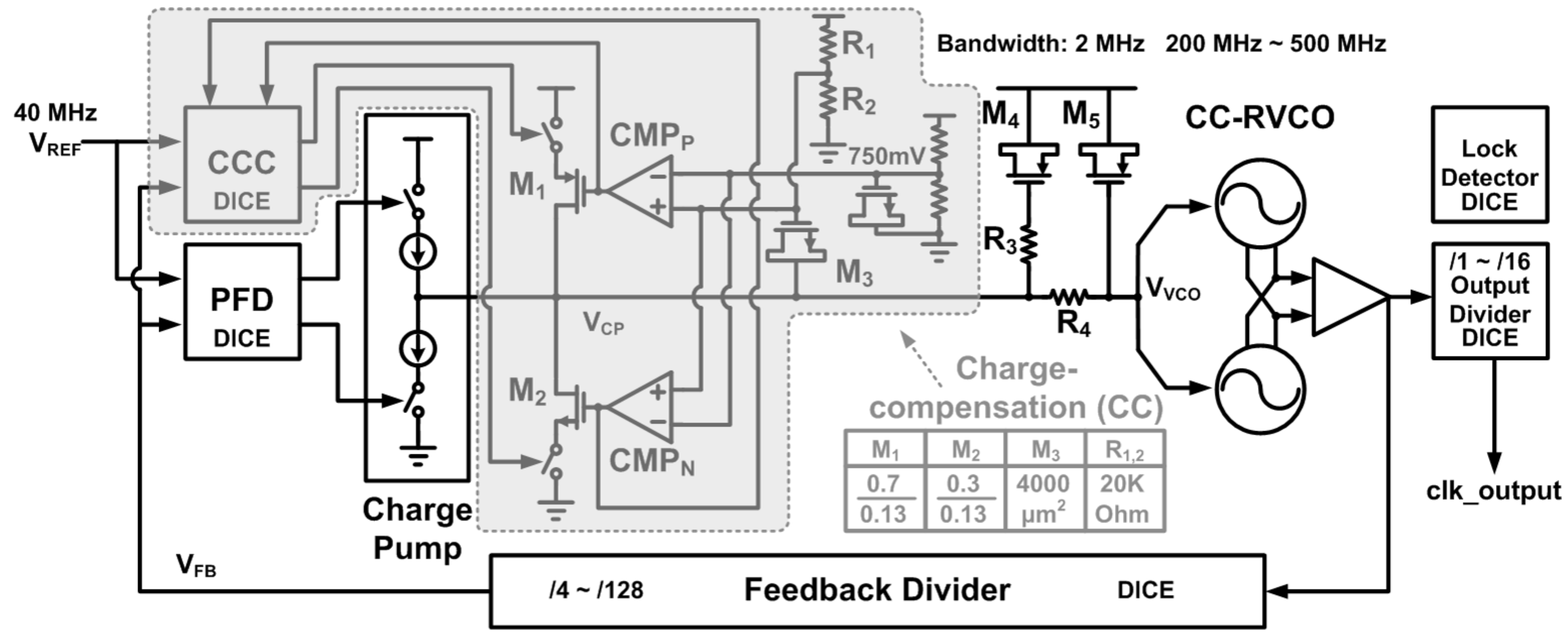
## Introduction

- The single event transient (SET) in PLLs disturbs analog signals at critical nodes and degrades PLL jitter performance.
- Research has proven that the output of charge-pump ($V_{CP}$) is the most SET sensitive node in a PLL [1]-[4].
- Mitigating SET effect at $V_{CP}$ can significantly reduce the PLL sensitivity to SET.
- This poster presents a new SET-induced charge detection and compensation technique to desensitize the PLL from SET at $V_{CP}$.
- This solution does not affect original PLL design.
- It improves both SET-induced VCO control voltage perturbation and recovery time.
- A control block is included to avoid the conflict between charge compensation and normal PLL phase correction.

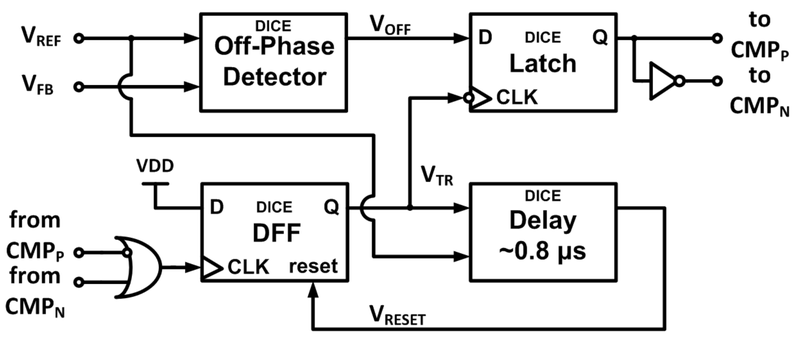
## Proposed PLL with SET-induced charge detection and compensation technique



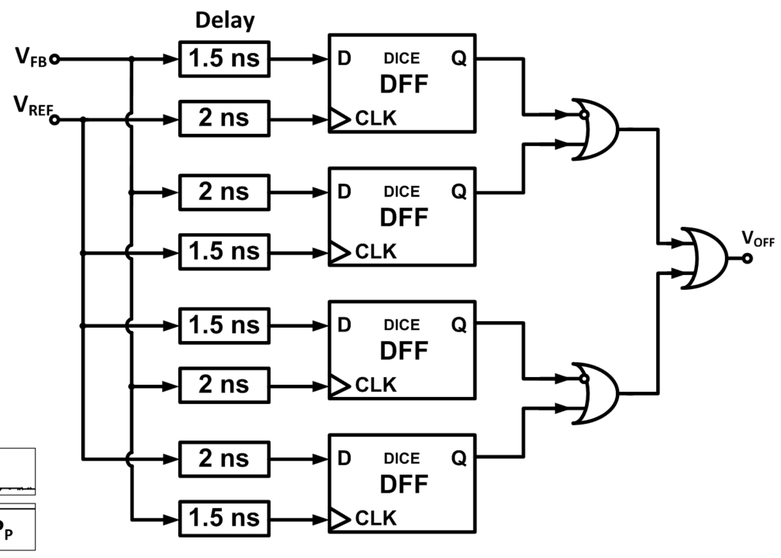

**PLL block diagram**

- Charge-compensation (CC) consists of three blocks: SET detector, compensator, and charge-compensation-controller (CCC).
- The SET detector includes two high-speed comparators, $CMP_P$ and $CMP_N$, as well as their biasing circuitries.
- The compensator comprises $M_1$, $M_2$, and two switches.
- The CCC generates control signals for switches to enable or disable the compensator.
- In normal operation, M1 and M2 are both turned off; switches in the compensator are turned on . Therefore, CC does not affect PLL operation but it is able to react to SET immediately.
- Once SET hits$V_{CP}$, the voltage perturbation is sensed and amplified to the digital level by $CMP_P$ or $CMP_N$. According to the polarity of the strike, either M1 or M2 will be turned on to compensate the injected charge.

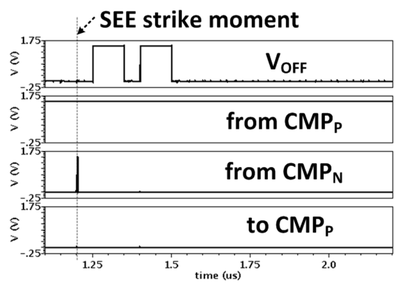
## Proposed charge-compensation-controller (CCC)



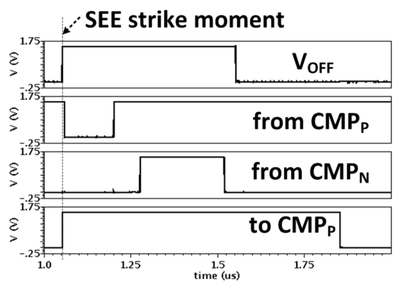

**CCC block diagram**




**Off-Phase detector block diagram**




**CC is enabled when SET hits $V_{CP}$**

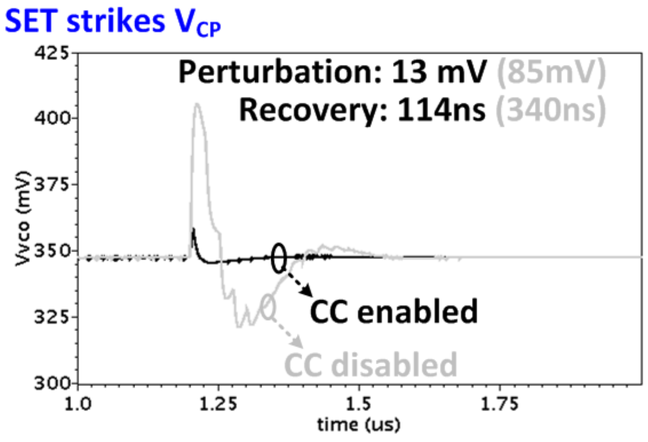



**CC is disabled with a reference phase step**

- The purpose of CCC is to avoid the conflict between charge compensation and normal PLL phase correction by guaranteeing that only SET happens at Vcp can CC be enabled. Otherwise, it is disabled.
- The principle of CCC is to monitor two incidents: input phase error and Vcp disturbance. If Vcp disturbance happens before there is input phase error, CCC enables the charge compensation scheme.

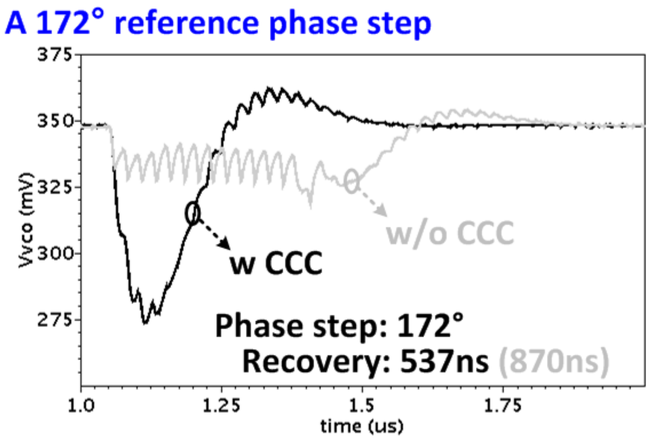
## Simulation Results

**SET strikes $V_{CP}$**



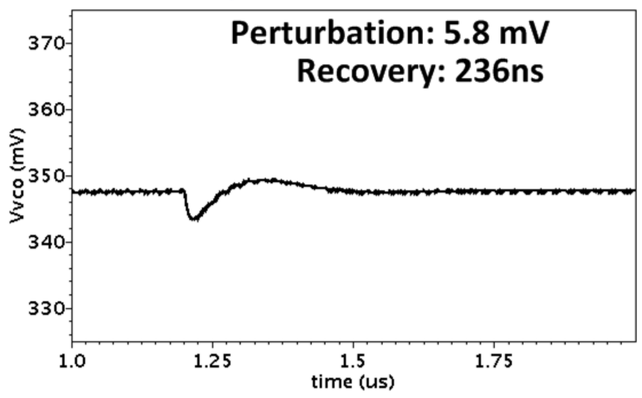

**(a) effectiveness of CC**

**A 172° reference phase step**

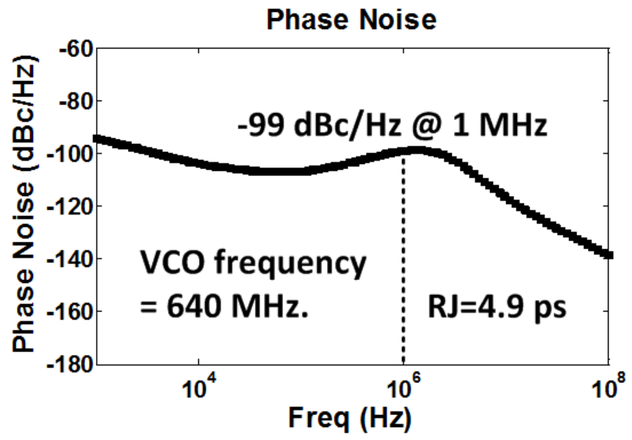



**(b) effectiveness of CCC**

**SET strikes output of $CMP_N$**




**(c) SET sensitivity of CC**




**(d) phase noise**

- (a) SET strikes $V_{CP}$ w/ and w/o CC when $V_{VCO}$ is around 350mV; CC can improve the voltage perturbation by a factor of 4 and reduce the recovery time by a factor of 3.
- (b) A 172° phase error step is introduced by multi-node ion strikes in the feedback divider w/ and w/o CCC; CCC successfully disable CC so that PLL can relock normally and faster
- (c) SET strikes the output of $CMP_N$; the $V_{VCO}$ disturbance is much less than that induced by SET at $V_{CP}$, meaning CC does not introduce more SET sensitive node to the PLL
- (d) Phase noise and integrated jitter; 4.9ps integrated jitter is achieved.

## Summary of the Proposed PLL Performance

| | |
|---|---|
| Process | 0.13 μm LP CMOS |
| Architecture | Type II Analog Ring VCO PLL |
| Area | 0.66×0.83 $mm^2$ |
| Supply Voltage | 1.5 V |
| Power Consumption | 21.5 mW |
| Tuning Range | 12.5 MHz ~ 500 MHz |
| $RJ_{RMS}$ | 4.7 pS |
| SEE Solution | CC, DICE, CC-RVCO, 3th order LP |
| CC Area | 0.22×0.13 $mm^2$ |
| CC Power Consumption | 4.5 mW |
| Device | Nominal VT transistor, Unsalicided P+ poly resistor |

## Reference


- [1] A.V. Kauppila *et al*., *RADECS* 2009, pp. 201–206.
- [2] S. Sondon *et al*., *LATW 2013,* pp. 1–5.
- [3] D. Matsuura *et al*., *RADECS 2011* pp. 150–155.
- [4] H. H. Chung *et al*., *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3539–3543, Dec. 2006.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