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SET Detection and Compensation and Its Application in PLL Design

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We present a new charge-compensation (CC) scheme to mitigate single-event-transient effect in designing a phase-locked loop. The CC method significantly reduces SET-induced voltage perturbation at the oscillator control node as well as a faster recovery. It is triggered only when SET strikes occurs and thus does not affect normal PLL dynamics. The PLL achieves a 12.5MHz to 500MHz tuning range with an RMS jitter of 4.9pS. It consumes 21.5mW of power under 1.5V supply. The CC circuit consumes 4.5mW of power and occupies 5.3% of the PLL area.

Summary

For applications in radiation environment, it is challenging to design a PLL due to single-event effects. SEE will cause single event upset (SEU) and single event transient (SET). SEU changes the state of sequential logic blocks; SET, on the other hand, disturbs analog signals at critical nodes. Although SEU can be effectively eliminated by using dual-interlock cell (DICE) flip-flops, SET is difficult to mitigate when it occurs in analog circuits and oscillators within a PLL. The output of charge pump (VCP) is the most SET-sensitive node. A small voltage perturbation along with a high VCO gain can lead to a significant frequency disturbance and jitter.

We propose a SET-induced charge detection and compensation technique. This solution does not affect typical PLL dynamics. It reduces both SET-induced VCO control voltage perturbation and improves PLL recovery time without introducing additional SET-sensitive nodes. A control block is also designed to avoid the conflict between CC compensation and normal PLL phase correction. The CC consists of three sub-blocks, SET detector, compensator, and charge-compensation-controller (CCC). The SET detector includes two high-speed comparators as well as their biasing circuitries. In normal operation, when the loop is locked and there is no SET, CCC will enable the compensator to be in standby mode so that it can react to SET immediately. If SET hits VCP, the voltage perturbation will be sensed and amplified and the compensator be turned on to compensate the injected charge. The solution comes with reasonable power, area, and performance cost.

A PLL with the proposed CC scheme is designed in a low-power 130nm digital CMOS technology. Besides the CC technique, all the sequential logic blocks are implemented using DICE cells. The timing parameters of the DICE cells are optimized to make it immune to SET at their input nodes. In addition, a cross-coupled ring VCO is developed to mitigate SET inside the VCO. With a 500 fC double-exponential current pulse injected at VCP, simulation results show the proposed CC method improves the voltage perturbation by a factor of 4 and reduces the recovery time by a factor of 3. Simulation results also indicate that with the charge-compensation-controller turned on the phase correction is much smoother and faster; while without CCC, the charge compensation will counteract the loop correction, which results in a 60% longer recovery time. When injecting a SET strike at the compensator output node, the voltage perturbation due to CC is much smaller than that caused by a SET at VCP indicating that the CC circuit does not introduce additional SET-sensitive nodes to the PLL.

The PLL achieves a 12.5MHz to 500MHz tuning range with an RMS jitter of 4.9pS. It consumes 21.5mW of power under 1.5V supply. The CC circuit consumes 4.5mW of power and occupies 5.3% of the PLL area. The jitter due to the CC circuit is about 0.2pS.

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