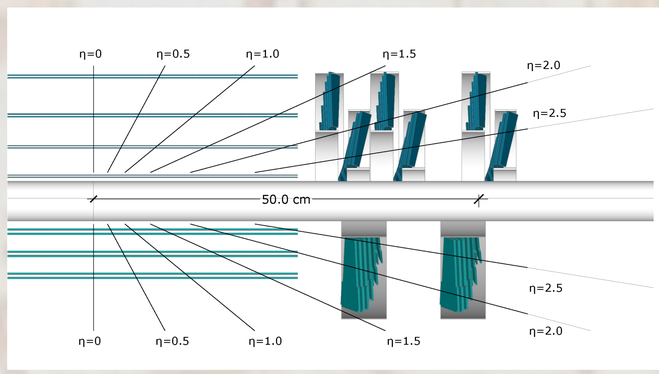
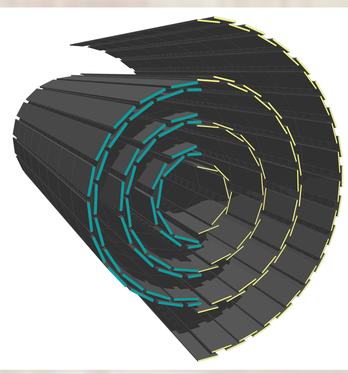
A digital readout system for the CMS Phase I Pixel Upgrade

Robert Stringer on behalf of the CMS Phase I Pixel Group

The Phase I Upgrade to the CMS Pixel Detector at the LHC features a new 400 Mb/s digital readout system. This new system utilizes upgraded custom ASICs, PSI46digv2.1 Read Out Chips (ROC) and Token Bit Manager (TBM) for data packaging, new optical links and changes to the Front End Drivers (FEDs). We will be presenting the new architecture of the full readout chain, the new schema for data encoding/transmission, and the results of preliminary testing of the new components.

The CMS Phase I Pixel Detector

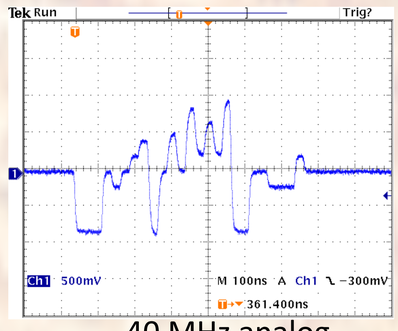




The CMS Phase I Pixel Upgrade will replace the current CMS Pixel Detector in 2017. The upgraded detector has four barrel layers and three forward disks, compared with three and two in the current detector. The detector will have twice the number of modules which must be read out using the same optical fiber infrastructure without adding new fibers.

Digital vs Analog

The current CMS Pixel Detector uses a 40 MHz digitally encoded analog signal. The modules for the upgraded detector have 16 digital readout chips (ROCs), PSI46digv2.1, which operate at 160Mb/s. An upgraded Token Buffer Manager (TBM) chip interleaves signals from two streams of 8 ROCs each into a 320 Mb/s stream and then encodes the data into a 400 Mb/s stream which is sent from the module.



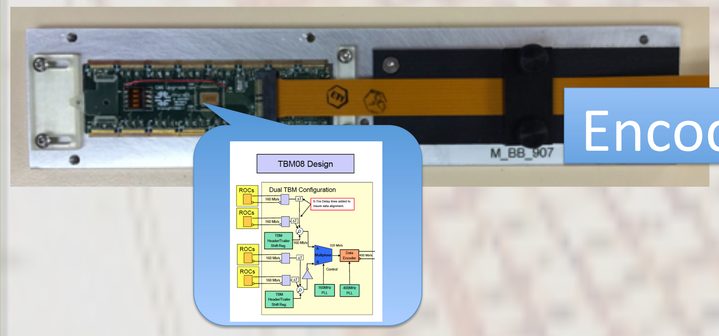
40 MHz analog

400 Mb/s digital

The CMS Phase I Pixel Readout Chain

The electronic signals travel to a port card located in the detector which contains a pixel optohybrid (POH) which contains a digital level translator (DLT) and an optical driver. The signals travel from the detector on optical fibers to the front end drivers (FED). The FEDs have optical receivers which operate most efficiently at higher speeds. The data encoding at 400 Mb/s is chosen so as to provide the receivers with a steady stream of approximately equal numbers of 0's and 1's to help minimize errors. The Pixel FED contains custom firmware for decoding and parsing the incoming pixel data. The prototype FED is based on the current Pixel FED with an additional daughter card for decoding the digital signal.

Module



Encoded Data

POH

Optical Data

FED

Constructing the 400 Mb/s Signal

Data

When ROCs are idle, 1s are continually sent.

Each event begins with a TBM header and ends with a TBM trailer.

Data Markers
H:011111111100
T: 011111111110

Error Detection

Each four bit word is mapped to a five bit word. This sparse mapping provides a method for identifying encoding/ decoding errors.

4-bit	5-bit
1001	→ 10011

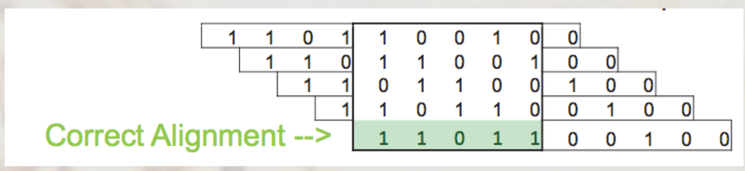
Optimization

Non-Return to Zero Inverted (NRZI) encoding is used to reduce errors in transmission by maximizing the number of high/low transitions. Encoded values depend on a preceding 0 or 1.

5-bit	NRZI
0 10011	→ 11101
1 10011	→ 00010

Data Alignment

As data is encoded in discrete five bit words, it is necessary to correctly identify the start of each word in the continuous data stream.



Special “framing” patterns which replace two values in the data stream allow for the start of the word to be easily identified. Since the all 1s and all 0s values cannot appear anywhere else in the data, there is only one possible alignment choice for these values.

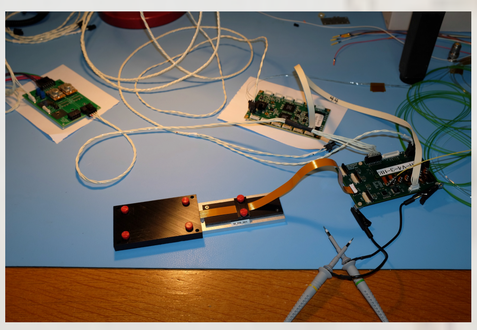
…11100**11111**0001100110111010**00000**..

↑ ↑

Frame is reset every time the pattern is detected.

Full Chain Tests

Tests of the full readout chain have been performed at CERN. Prior to the production of prototype components, preliminary tests involved a simulated data stream decoded by FED with Zarlink receiver. Over 500k simulated events were decoded without error representing a bit error rate < 10^{-8}.

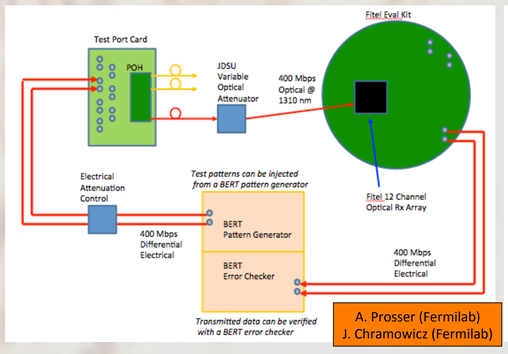


The first full Phase I Pixel readout chain using prototype components.

Upgraded Pixel FED w/two daughterboards and controllers.

POH Bit Error Rate Tests

Error rates are required to be less than 10^{-12} and expected to be less than 10^{-15}. Measuring the error rate directly at 400 Mb/s would not be practical, at 10^{-15} one error would occur every 11.6 hours! To measure the rate faster, the signal is attenuated and the error rate is extrapolated. The extrapolated error rate was shown to be less than 10^{-12}.



A. Prosser (Fermilab)
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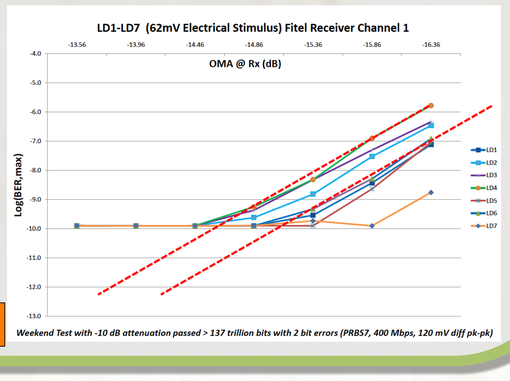

Weekend Test with -10 dB attenuation passed > 137 trillion bits with 2 bit errors (PRBS7, 400 Mbps, 120 mV diff pk-pk)

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