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A Digital Readout System for the CMS Phase I Pixel Upgrade

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The Phase I Upgrade to the CMS Pixel Detector at the LHC features a new 400 Mb/s digital readout system. This new system utilizes upgraded custom ASICs, PSI46dig Read Out Chips (ROC) and Token Bit Manager (TBM08/09) for data packaging, new optical links, and changes to the Front End Drivers (FEDs). We will be presenting the new architecture of the full readout chain, the new schema for data encoding/transmission, and the results of preliminary testing of the new components.

Summary

The data acquisition system of the CMS Phase I Pixel Detector will be required to read out pixel hits at trigger rates exceeding 100 kHz, in the high pileup conditions at the LHC. The new PSI46digV2.1 Read Out Chip (ROC) was designed to address the inefficiencies in the current ROC experienced during high luminosity running at the end of 2013.

The new digital ROC, unlike the previous analog ROC, outputs binary data at 160 Mb/s. The Token Bit Manager (TBM) combines two parallel data streams from several ROCs into a 320 Mb/s stream and packages the ROC data into discrete events by prepending/appending unique header and trailer signals that also contain additional status information. The final output is converted using 4 to 5 bit and Non Return to Zero Inverted (NRZI) methods, for DC level balancing, to create a 400 Mb/s data stream.

The encoding scheme was designed to minimize transmission errors. The 4-5 bit encoding creates distinct 5-bit words in the binary data stream, which must remain synchronized in the decoder. To set and correct the "framing" of the data words, one of the 16 used values is replaced by a "framing pattern" that can be used to align the data in the decoder. This framing replacement is made continuously during output.

The final binary data stream is transferred to the Front End Driver (FED) using optical links. Each component of this readout chain was tested individually, building up to a full chain test as components became available.

The full readout chain can be divided into three major components: modules, opto-hybrids, and FEDS. The modules, which contain the ROCs and TBMs, have different configurations depending their location in the detector. Each module has 16 ROCs that are read out in groups of 8 (4 for higher rate areas) in each output data stream. These modules were tested using injected calibration signals as well as with pixel hits from direct x-rays. The 400 Mb/s data stream was successfully decoded using both methods, with the x-ray data showing a complete image of the module.

The optical signal from the Pixel OptoHybrid (POH) was tested using a bit error rate tester. The error rate was calculated at several levels of optical attenuation. These values were then used to extrapolate the error rate of the full strength signal. The extrapolated value was determined to be less than 10-12.

Two designs were considered for the Upgrade Pixel FED. The first design modifies the current VME Pixel FED, replacing the optical receiver and decoding FPGAs with a 400 Mb/s deserializer daughterboard. The first prototype FEDs were tested using a module emulator connected to the POH, and showed an error rate of less than 10-8.

The second design changes from VME to uTCA architecture, and also changes the FPGAs from Altera to Xilinx. The uTCA FED was still under development and was not available for testing.

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